CRD49530 -USB
Customer Reference Design

CRD49530-USB

User's Manual

Preliminary Product Information

This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.

To find the one nearest to you go to **www.cirrus.com**

Contents

Figures

Tables

Chapter 1

Kit Contents and Requirements

1.1 CRD49530-USB Kit Contents

Each CRD49530-USB kit comes with the following:

- CRD49530 Development Board
- Power Supply: +9V, 1.67A, 100V - 240V with AC Power Cord
- CRD USB Master USB Digital I/O Card
- USB Cable
- Document Card explaining how to get the latest board software

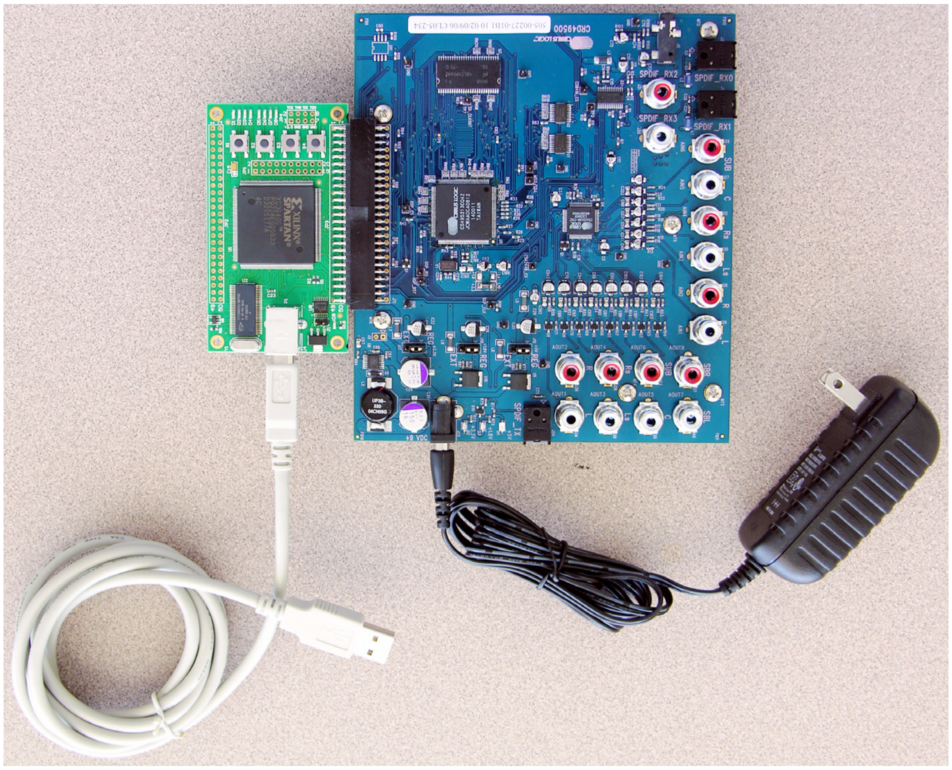


Figure 1-1. CRD49530 Kit Contents

1.2 Requirements

1.2.1 PC Requirements

- Microsoft Windows® XP Operating System
- USB 2.0 Support

1.2.2 Software Requirements

- Cirrus Evaluation Software Package (available from your local Cirrus Logic representative)

1.2.3 Support Hardware Requirements

- Digital or Analog Audio Source (e.g. DVD player, PC with a digital audio card/device)
- Amplified Speakers for audio playback (e.g. powered PC speakers, AVR/amp + speakers)

1.2.4 Cabling Requirements

- Digital Audio Inputs – S/PDIF Optical Cables, RCA Audio cables (Connect to digital audio card, audio analyzer, or DVD player.)
- Digital Audio Output – S/PDIF Optical Cables (Connect to digital audio card, audio analyzer, or AVR.)
- Analog Audio Inputs – RCA Audio Cables (Connect CRD49530 line-level inputs to analog audio source.)
- Analog Audio Outputs – RCA Audio Cables (Connect CRD49530 line-level outputs to powered speakers.)

1.3 CRD49530-USB System Description

A detailed block diagram of the CRD49530-USB Customer Reference Design is shown below in Figure 1-2. The sections that follow provide a detailed description of each block.

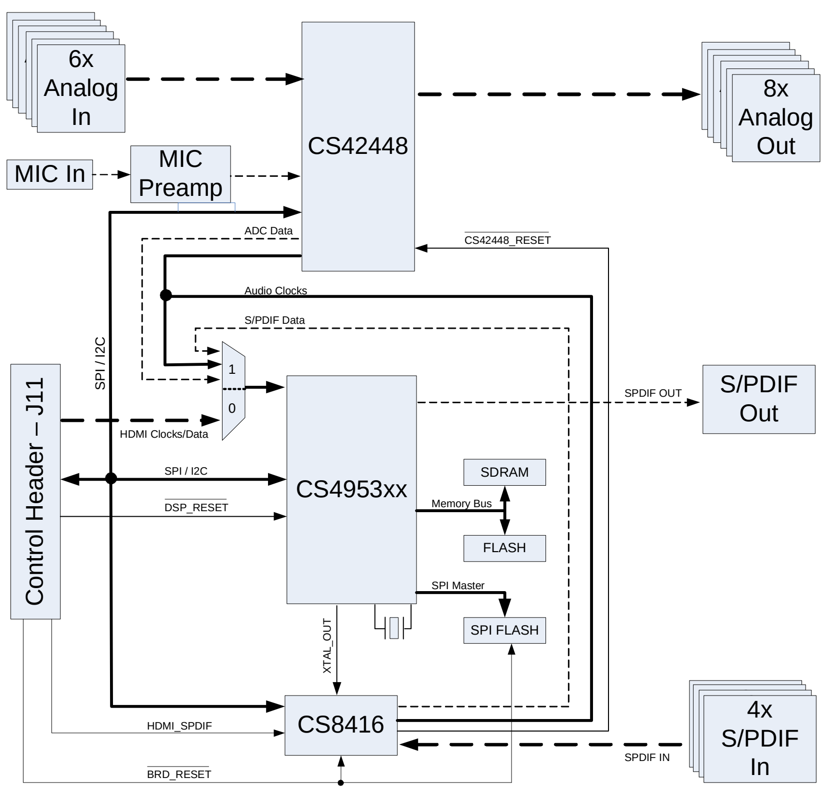


Figure 1-2. CRD49530-USB Block Diagram

1.3.1 Audio Inputs

1.3.1.1 Analog Line-level Inputs

- Connector Type: RCA Female
- Absolute Maximum Signal Level: +6.5V
- Absolute Minimum Signal Level: GND - 0.7V
- Full Scale Amplitude: $2V_{RMS}$
- Reference Designators: J12, J26-J30, or AIN1 - AIN6

1.3.1.2 Optical Digital Inputs

- Connector Type: Fiber Optic RX for Digital Audio, JIS F05 (JIS C5974-1993 F05)
- Reference Designators: J1-J2, or SPDIF_RX0-SPDIF_RX1

1.3.1.3 Coaxial Digital Inputs

- Connector Type: RCA Female
- Maximum Signal Level: +3.3V
- Minimum Signal Level: GND - 0.7V
- Reference Designators: J31-J32, or SPDIF_RX2-SPDIF_RX3

1.3.1.4 Microphone Input

- Absolute Maximum Signal Level: +5V
- Absolute Minimum Signal Level: GND - 0.7V
- Full Scale Amplitude: 7mVp-p
- Reference Designator: J5

The microphone preamplifier shares the AIN5 ADC with the AIN5 RCA jack. Only one analog source can be sampled at any given time. When the microphone input is selected, the AIN5 audio jack is ignored. The default configuration enables the AIN5 audio jack.

1.3.2 Audio Outputs

1.3.2.1 Analog Line-level Outputs

- Connector Type: RCA Female
- Full Scale Amplitude: $1.21V_{RMS}$
- Reference Designators: J33-J40, or AOUT1 - AOUT8

1.3.2.2 Optical Digital Output

- Connector Type: Fiber Optic TX for Digital Audio, JIS F05 (JIS C5974-1993 F05)
- Reference Designator: J24, or SPDIF_TX
- The S/PDIF output uses the same data line as AOUT7 and AOUT8. When the digital output has been enabled, and you have speakers connected to AOUT7 and AOUT8 white noise will be heard. This could damage the speakers.

1.3.2.3 DC Power Input

- Voltage Range: +9VDC TO +12VDC
- Minimum Power: 8W supply
- Connector Type: 2mm Female, positive center pin
- Reference Designator: J25

1.3.3 Control Header

- Connector Type: 2x25, 0.100 inch Shrouded Male
- Reference Designator: J11

This connector is the interface between the CRD49530 and the CRD USB Master. Control signals, clocks, data, and +3.3V power are passed across this connector.

1.3.4 On-Board Voltage Selection Headers

- Connector Type: 1x3, 0.100 inch, Stake Header
- Reference Designator: J17 - J19

The CRD49530-USB is designed to operate from a single DC power input. The 9V power supply provided with the kit is connected to the DC power input jack (J25) and is regulated down to the system voltages (5V, 3.3V, 1.8V). The power selection headers should be set to the 'REG' position when using the DC wall supply. This is the default mode of operation and should not need to be changed for most applications.

It is possible to bypass the regulated power supplies for any of the voltages by removing the jumper from the appropriate power selection header, and connecting an external voltage supply to the center pin of that selection header.

The third configuration for the power selection headers is the 'EXT' position. This is a special mode of operation, and cannot be used while connected to the CRD USB Master control board. Placing the power selection headers in the 'EXT' position while connected to the CRD USB Master will prevent the board from operating.

The unpopulated header, J3, is also designed for a special mode that brings 12V from the control header, but cannot be used when connected to the CRD USB Master.

1.3.5 Audio Input Source Multiplexer

- Source 0: CRD USB Master USB Board (This feature is used by engineering development and debugging purposes.)
- Source 1: CS8416 and CS42448
- Reference Designators: U1, U2

This multiplexer is used to select which audio sources feed the CS4953xx DAI pins. When the on-board sources (CS8416, U3 and CS42448, U4) are being used, the CRD USB Master data cannot be processed. Likewise, when the HDMI source (CRD USB Master) is selected, the on-board audio inputs are disabled.

1.3.6 CS4953xx Audio DSP

The CS4953xx audio DSP (U5) are a family of dual-core processors designed specifically for audio applications. The CRD49530 allows a designer to evaluate the CS4953xx DSPs in many different modes of multi-channel input and output. The 144-pin footprint on this board is compatible with any CS4953xx (or CS497xx) chip that uses the LQFP144 package.

Audio input data to the DSP can come from any of the following sources:

- CS8416 (U3)
- CS42448 (U4)
- CRD USB Master (feature not currently supported)
- Audio output data from the DSP can be sent to the following destinations:
- CS42448 for conversion to Analog Output (AOUT1 - AOUT8)
- Optical S/PDIF Out (SPDIF_TX), this option disables AOUT7 and AOUT8

The CS4953xx has many applications stored in internal ROM, but a host is still required to configure the application for a particular system. The CRD49530 allows the PC to act as a host to boot and configure the DSP through the GUI software.

The CS4953xx can also be booted from external serial flash for custom applications that are not stored in the DSP's ROM.

Note: The 144-pin footprint on this board is also compatible with the CS495xx family of DSPs. The CRD49530 can support any CS495xx chip if the alternate stuffing options shown on the DSP schematic page have been followed.

1.3.7 CS8416 S/PDIF RX

The CS8416 (U3) is a 192 kHz S/PDIF receiver with an integrated input multiplexer. All of the S/PDIF input jacks (RX0-RX3) are connected to the CS8416. The active S/PDIF jack is selected by changing the internal mux through the serial host port of the CS8416. This selection is controlled through the Audio In configuration within DSP Composer (see Chapter 4 for details).

When S/PDIF audio is being processed, the CS8416 must master MCLK for the system (see "Audio Clocking" on page 1-6 for details).

1.3.8 CS42448 Audio Codec

The CS42448 (U4) is a high-performance, multi-channel audio codec capable of supporting sample rates up to 192 kHz on its 6 ADCs and 8 DACs. This device is used for all analog-to-digital and digital-to-analog conversions on the CRD49530.

All analog inputs (AIN1-AIN6) and all analog outputs (AOUT1-AOUT8) are connected to the CS42448. The microphone input shares the AIN5 ADC with the AIN5 RCA jack. When the microphone is in use, the AIN5 RCA jack is ignored.

When analog audio is being processed, the 24.576 MHz crystal for the CS4953xx must master MCLK for the system (see "Audio Clocking" on page 1-6 for details).

1.3.9 Memory

The CRD49530 is populated with a 4 Mbit serial flash. There are 2 footprints (U11, U13) on the board for compatibility with both standard 8-pin serial flash pinouts. The serial control lines are shared by both footprints. Only one serial flash chip can be populated.

The CS4953xx can use external SDRAM (U7) to implement features such as large multi-channel audio delays. A 64 Mbit SDRAM (166 MHz) is connected to the 150 MHz memory bus of the CS4953xx.

There is an additional unpopulated footprint for a parallel flash (U6) memory device. This device was routed on the board as an example of how to route the memory bus when using a parallel flash memory,

but Cirrus recommends using serial flash for all systems. Adding a parallel flash makes the routing of the SDRAM bus much more complicated.

1.3.10 Audio Clocking

Clocking architecture is one of the most important aspects of an audio system. The input and output clock domains of the DSP must be synchronous when delivering audio data in an isochronous fashion (constant bitrate delivery), even if the input/output domains operate at different frequencies (e.g. 48 kHz input/96 kHz output). Systems utilizing I^2S delivery of S/PDIF input, ADC input, or other digital audio input use isochronous delivery.

The requirements are slightly more complicated for systems using “bursty” delivery on the input side of the DSP, but the CRD49530 is designed to emulate isochronous systems.

The CRD49530 can operate in three different clocking modes. Each of these modes is explained in the following sections.

1.3.10.1 Clock and Data Flow for ADC Input

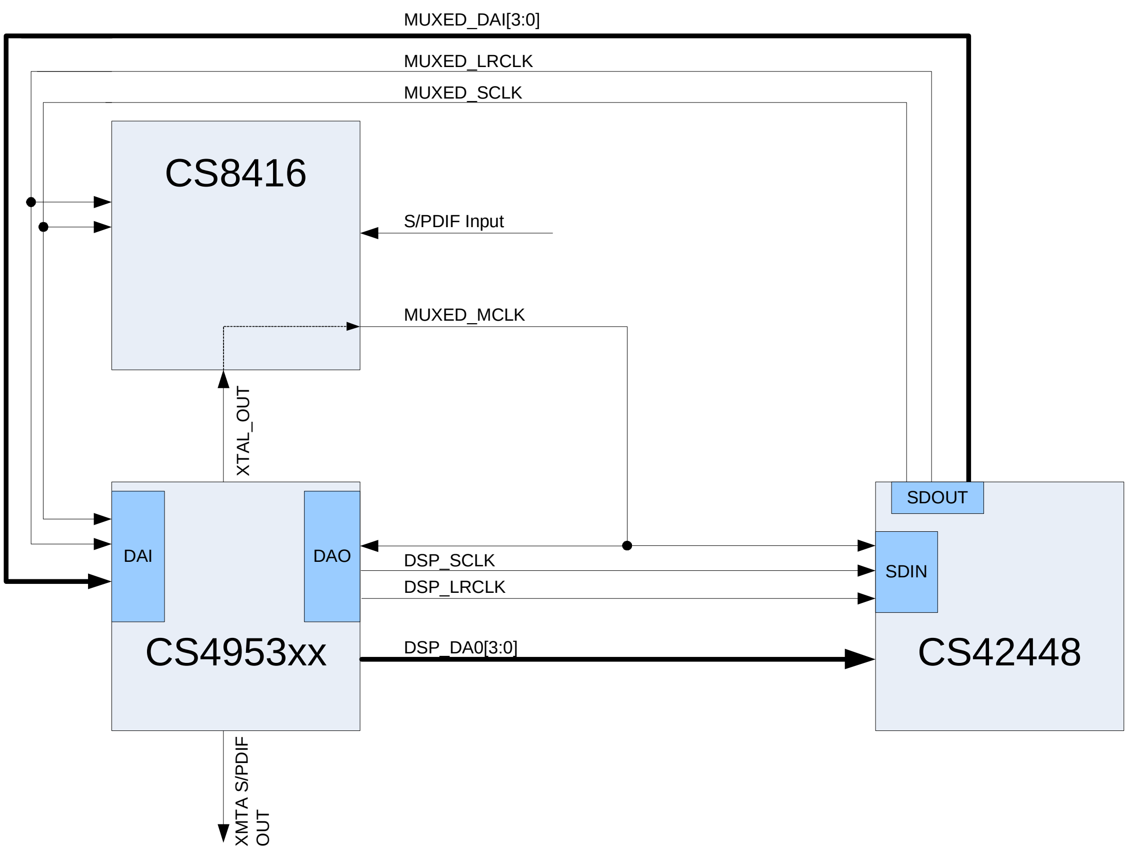


Figure 1-3. ADC Clocking

The ADC clocking architecture is used when the ADCs are used as the only audio input (i.e. S/PDIF is disabled as described in "USB (I2S) Audio Input" on page 4-5), and the audio input source multiplexer (U1, U2) is used to select on-board audio sources. Figure 1-3 illustrates this clocking configuration.

XTAL_OUT from the CS4953xx is MCLK for the system, and the codec masters the input clocks (MUXED_SCLK/MUXED_LRCLK) of the CS4953xx. The system routing of the clocks was simplified by using the CS8416 to drive MCLK to the system, but the internal clock multiplexer of the CS8416 is forced to the OMCK setting to pass XTAL_OUT.

The CS4953xx always masters its output clocks (DSP_SCLK/DSP_LRCLK).

Table 1-1. ADC Clocking

Clock Name	Clock Master Source	Clock Driver	Clock Frequency
MUXED_MCLK	CS4953xx	CS8416	24.576 MHz
MUXED_SCLK	MUXED_MCLK	CS42448	64*Input Fs (default)
MUXED_LRCLK	MUXED_MCLK	CS42448	Input Fs
DSP_SCLK	MUXED_MCLK	CS4953xx	64*Output Fs (default)
DSP_LRCLK	MUXED_MCLK	CS4953xx	1*Input Fs (default)

Note: MUXED_MCLK is the clock signal that is driven by the CS8416’s RMCK pin. The CS8416 provides the recovered clock from the S/PDIF input unless it loses signal lock, in which case the CS8416 passes the DSP clock (XTAL_OUT) that it receives on the OMCK pin.

1.3.10.2 Clock and Data Flow for S/PDIF Input

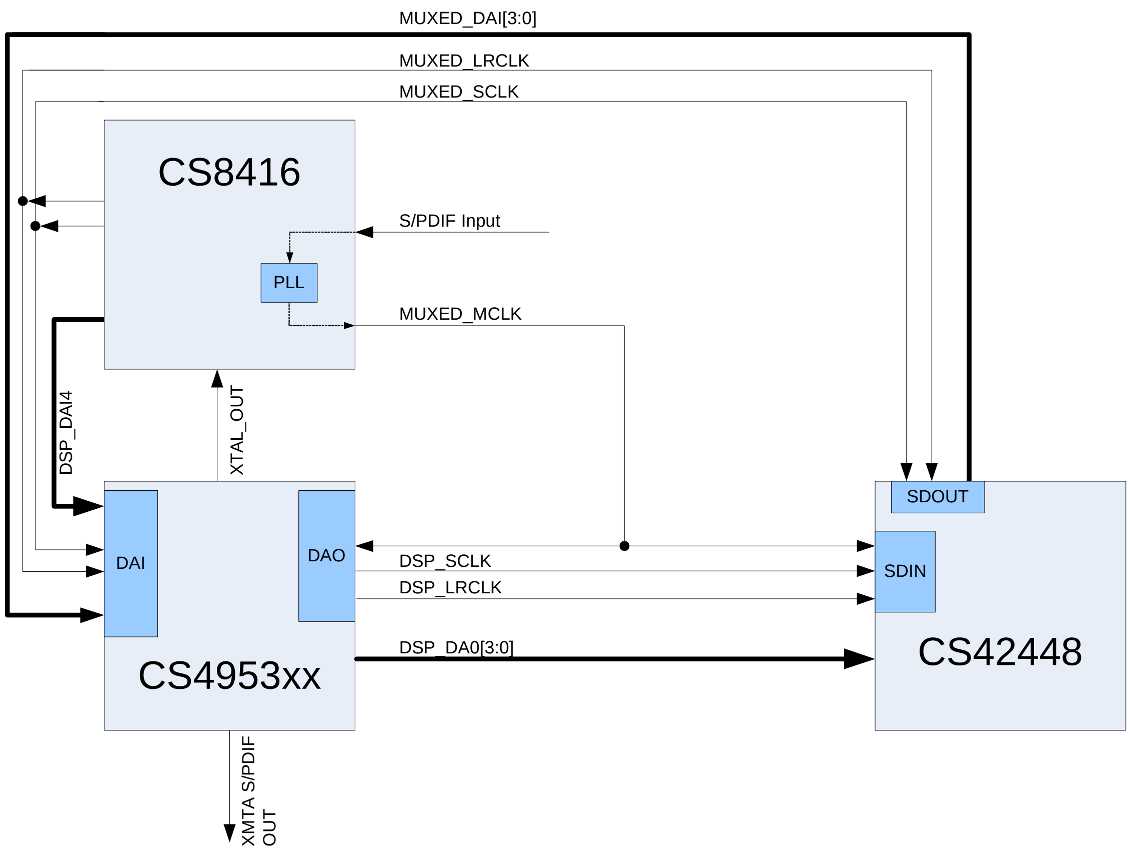


Figure 1-4. S/PDIF Clocking

The S/PDIF clocking architecture is used when any S/PDIF RX is used as an audio source, whether S/PDIF is the only audio input or is used at the same time as ADC audio (i.e. any S/PDIF RX is selected as described in "USB (I2S) Audio Input" on page 4-5), and the audio input source multiplexer (U1, U2) is used to select on-board audio sources. Figure 1-4 illustrates this clocking configuration.

MCLK recovered from the incoming S/PDIF stream must be MCLK for the system, and the codec masters the input clocks (MUXED_SCLK/MUXED_LRCLK) of the CS4953xx. In this configuration the internal multiplexer of the CS8416 routes the recovered MCLK to MUXED_MCLK.

The CS4953xx always masters its output clocks (DSP_SCLK/DSP_LRCLK).

Table 1-2. S/PDIF Clocking

Clock Name	Clock Master Source	Clock Driver	Clock Frequency
MUXED_MCLK	CS8416	CS8416	256*S/PDIF Fs (e.g. 12.288 MHz for 48 kHz)
MUXED_SCLK	MUXED_MCLK	CS8416	64*Input Fs (default)
MUXED_LRCLK	MUXED_MCLK	CS8416	Input Fs
DSP_SCLK	MUXED_MCLK	CS4953xx	64*Output Fs (default)
DSP_LRCLK	MUXED_MCLK	CS4953xx	1*Input Fs (default)

Note: MUXED_MCLK is the clock signal that is driven by the CS8416's RMCK pin. The CS8416 provides the recovered clock from the S/PDIF input unless it loses signal lock, in which case the CS8416 passes the DSP clock (XTAL_OUT) that it receives on the OMCK pin.

1.3.10.3 Clock and Data Flow for USB Data Delivery

This feature is used by engineering development and debugging purposes.

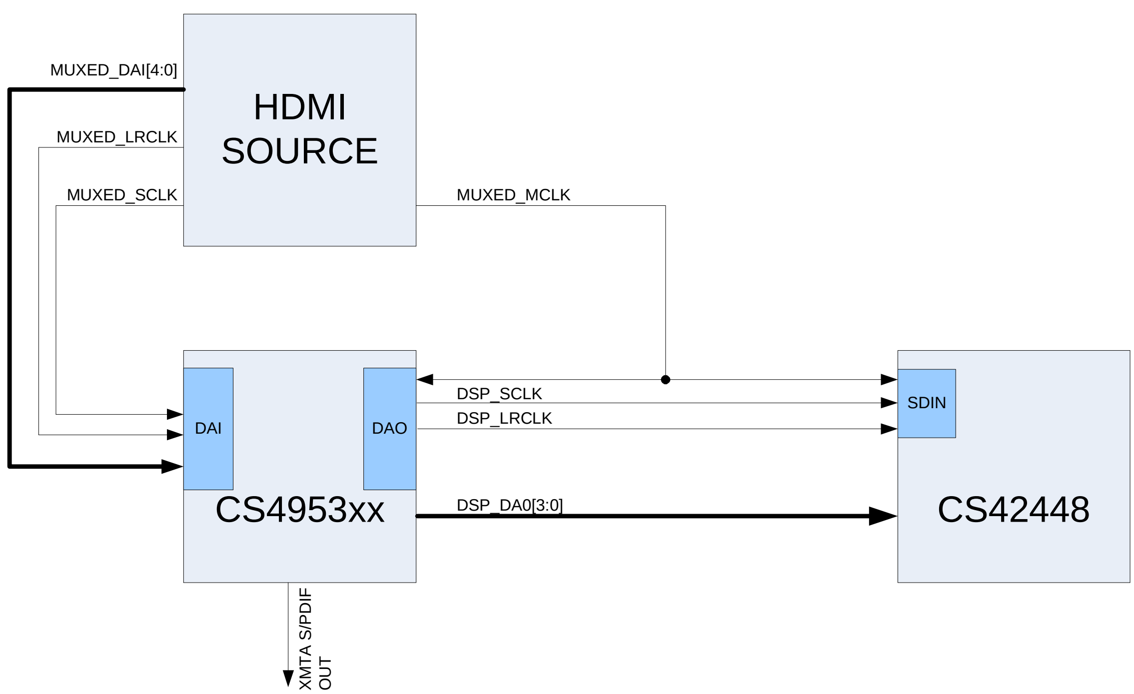


Figure 1-5. HDMI Clocking

When the audio input source multiplexer (U1, U2) is used to select HDMI clocks and data, the HDMI source masters the system MCLK, and the input clocks (MUXED_SCLK/MUXED_LRCLK) of the CS4953xx.

The CS4953xx always masters its output clocks (DSP_SCLK/DSP_LRCLK).

Table 1-3. HDMI Clocking

Clock Name	Clock Master Source	Clock Driver	Clock Frequency
MUXED_MCLK	HDMI® Source	HDMI Source	256*S/PDIF Fs (e.g. 12.288 MHz for 48 kHz)
MUXED_SCLK	MUXED_MCLK	HDMI Source	64*Input Fs (default)
MUXED_LRCLK	MUXED_MCLK	HDMI Source	Input Fs
DSP_SCLK	MUXED_MCLK	CS4953xx	64*Output Fs (default)
DSP_LRCLK	MUXED_MCLK	CS4953xx	1*Input Fs (default)

Note: MUXED_MCLK is the clock signal that is driven by the HDMI source.

1.4 Other Useful Information

1.4.1 Web Sites

- Cirrus Logic main web site: www.cirrus.com

1.5 Information Shipped with the Evaluation Kit

By installing `cs4953x_eval_kit.exe`, end users can access the information described in the followin subsections.

1.5.1 DSP Information

- *CS4953xx Data Sheet*
- *CS4953xx Hardware User's Manual*
- *AN288, CS4953xx / CS497xxxx Firmware User's Manual*

1.5.2 Board Information

- Schematics
- BOM
- Artwork and PCB stackup

1.5.3 Audio Codec Information

- *CS42448 Data Sheet*
- *CS42448 Errata*

1.5.4 S/PDIF Receiver Information

The following information is located on the www.cirrus.com web site.

- *CS8416 Data Sheet*
- *CS8416 Errata*

1.5.5 DSP Software Utility Information

- *DSP Composer User's Manual*

The documents listed above are updated periodically and may be more up-to-date than the information in this document. Check the Cirrus Logic web site for the latest updates.

§§[1]

1. The "§§" symbol is used throughout this manual to indicate the end of the text flow in a chapter.

Chapter 2

Introduction to CRD49530-USB Kit

2.1 Introducing the CRD49530-USB Customer Reference Kit

The CRD49530-USB kit is composed of the CRD49530 customer reference design and the CRD USB Master USB Control board. The CRD49530 provides a practical platform for emulating a typical multi-channel audio system application. The CRD USB Master is a USB control board used to interface the host PC to the CRD49530, and convert GUI commands into the serial control protocol required for configuring the CS4953xx, CS42448, and CS8416 audio ICs. Figure 2-1 shows the relationship between the CRD49530 and the CRD USB Master.

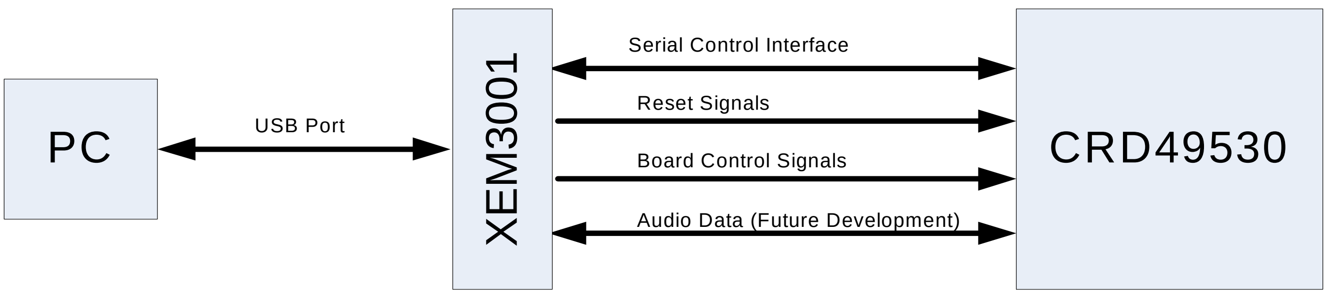


Figure 2-1. CRD49530-USB System Block Diagram

This document will concentrate on the features and basic operation of the CRD49530 board. Detailed information regarding the operation and programming of the CS4953xx DSP is covered by the *CS4953xx Data Sheet, CS4953xx Hardware User's Manual*, and application note AN288 (see "Other Useful Information"on page 1-9 for more details).

The CRD49530 is a convenient and easy-to-operate evaluation platform. It has been designed to demonstrate the majority of the CS4953xx functions on a small 6" x 5.5" base board. These features include:

- PC control of the CS4953xx using the DSP Composer™ graphical user interface
- Serial control of audio devices on CRD49530 via I²C® or SPI™ protocols
- Digital audio input of PCM or compressed data via optical or coaxial S/PDIF
- 6-channel analog audio input via the CS42448 audio codec
- 8-channel analog output through the CS42448 audio codec
- Digital audio output of PCM data via optical S/PDIF
- Multi-channel digital audio input via the USB Master (feature not currently supported)
- Separate input and output clocking domains to allow 1FS-to-2FS audio processing on the CS4953xx
- DSP Memory expansion through external 64 Mbit SDRAM
- Fast boot – host-controlled master boot (HCMB) of custom applications from 4 Mbit serial SPI flash device.
- Microphone input with integrated amplifier for Intelligent Room Calibration (IRC) evaluation
- Supports all members of the CS4953xx and CS497xx family in the 144-pin LQFP package.

Note: Not all features of the CS4953xx are exercised on the CRD49530.

2.1.1 Identifying Components on the CRD49530-USB

Figure 2-2 shows the top side of the CRD49530. The accompanying legend identifies the main components of the board.

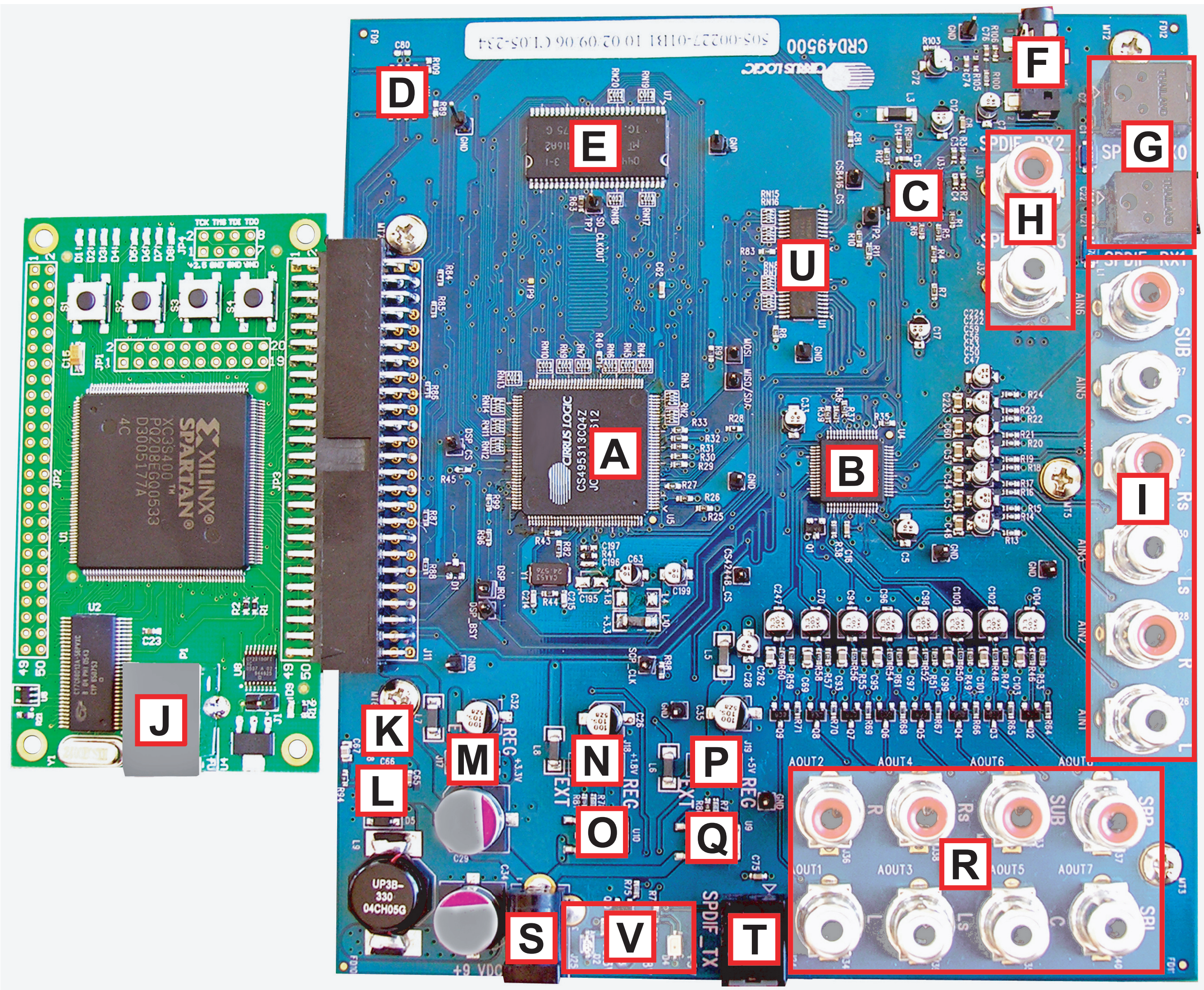


Figure 2-2. CRD49530 Top View

A. CS4953xx DSP, U5
B. CS42448 Audio Codec, U4
C. CS8416 S/PDIF Receiver, U3
D. 4 Mbit Serial Flash, U11
E. 64 Mbit SDRAM (166 MHz), U7
F. 1/8" Microphone Input Jack
G. Optical S/PDIF Input Jacks

H. Coaxial S/PDIF Input Jacks
I. Analog Inputs, 2 V_{RMS} Max
J. USB Connector on CRD USB Master
K. Alternate +12V Jumper, J3
L. +3.3V Switching Regulator (1.5A), U8
M. +3.3V Selection Header (Regulator/External), J17
N. +1.8V Selection Header (Regulator/External), J18
O. +1.8V Linear Regulator (1A), U10
P. +5V Selection Header (Regulator/External), J19
Q. +5V Linear Regulator (1A), U9
R. Analog Audio Outputs
S. DC Power Input Jack, +9V_{DC} to +12V_{DC}
T. Optical S/PDIF Output Jack
U. On-board/External Digital Audio Mux, U1 & U2
V. Power Indicator LEDs

§§

Chapter 3

Installation and Setup for Running Application

3.1 Installation, Setup, and Running First Application



It is important to install the latest Evaluation Software (`cs4953x_eval_kit.exe`) BEFORE connecting the USB cable from the PC to the CRD Master-USB daughter card. Failure to install the evaluation software before the initial connection can result in an inability to communicate with the CRD49530.

3.1.1 Evaluation Software Installation

The DSP evaluation software installation will first install the Cirrus Logic DSP evaluation software followed by the USB drivers required to communicate with the CRD USB Master.

1. Run the latest DSP evaluation software installation executable (`cs4953x_eval_kit_rcxx.exe`. This executable is supplied by your Cirrus Logic representative.
2. At the *Welcome* screen, click *Next.*
3. At the *Licensing Agreement* window, select the *"I accept the agreement"* radio button to agree to the terms and then select *Next.*
4. Select the *Destination Location* window, Select the default location *"C:\CirrusDSP"* and click *Next*.
5. Select *Start Menu Folder* window, Select the default location *"C:\CirrusDSP"* and click *Next*.
6. The *Ready to Install* window indicates the selected destination location and the *Start* menu folder for confirmation, select *Install* to begin the install process which should take less than one minute.
7. After the DSP evaluation software is installed, the installer will launch the *Front Panel Driver Setup Wizard* (below). Click *Next* to continue the installation.

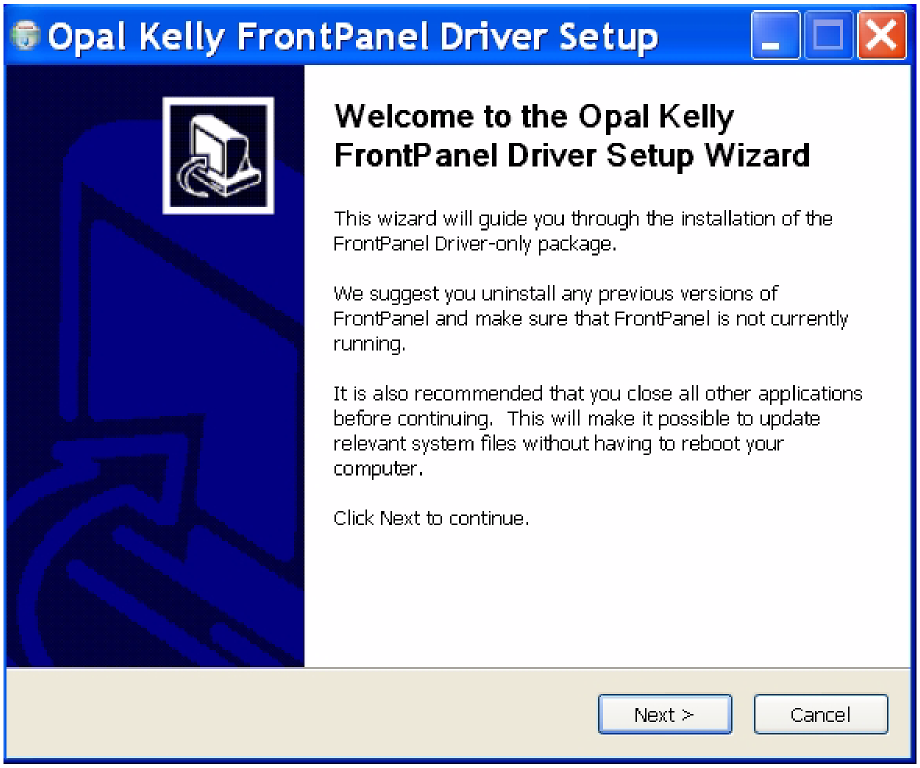


Figure 3-1. Front Panel Driver Setup Wizard

8. The *Opal Kelly Licensing Agreement* window will appear next. Click *"I Agree"* to agree to the terms and continue.
9. The next window asks the user to choose components for installation. By default, only one component is available and is pre-selected – *Unified USB Driver*. Click *Next* to continue.
10. The wizard will then ask the user to choose the install location. Select the default location of *"C:\Program Files\Opal Kelly\FrontPanel"* and click *Install*. This should take only a few seconds.
11. Click *Finish* once the wizard has completed installation of the drivers.
12. The Cirrus DSP evaluation software will then prompt the user to click *Finish* to exit the setup wizard.

3.1.2 Setting up the CS49530-USB Boards

1. Place the CRD49530 and the CRD USB Master on a static-free surface.
2. If the boards are not mated, connect them together as shown in Figure 3-2. Notice that the USB connector on the CRD USB Master and the power connector on the CRD49530 are on the same side.
3. Connect the power supply jack to the CRD49530 board at J25 and the adapter to a wall power socket or power strip.
4. Check that the D3 (green), D2 (red), and D4 (orange) power indicator LEDs illuminate on the CRD4953x.
5. Make Audio Input connections to the to CRD49530 baord
   - Connect one end of the digital audio S/PDIF optical cable to SPDIF_RX0 on the CRD49530 board.

- Connect the other end of the optical cable to the optical output on the back of a DVD player or other digital audio source.

6. Make Audio Output connections from the CRD49530 board.
   - The RCA connectors labeled AOUT1 and AOUT2 are the left and right analog output channels.
   - Use the RCA audio cables to connect these line-level analog outputs to powered speakers.

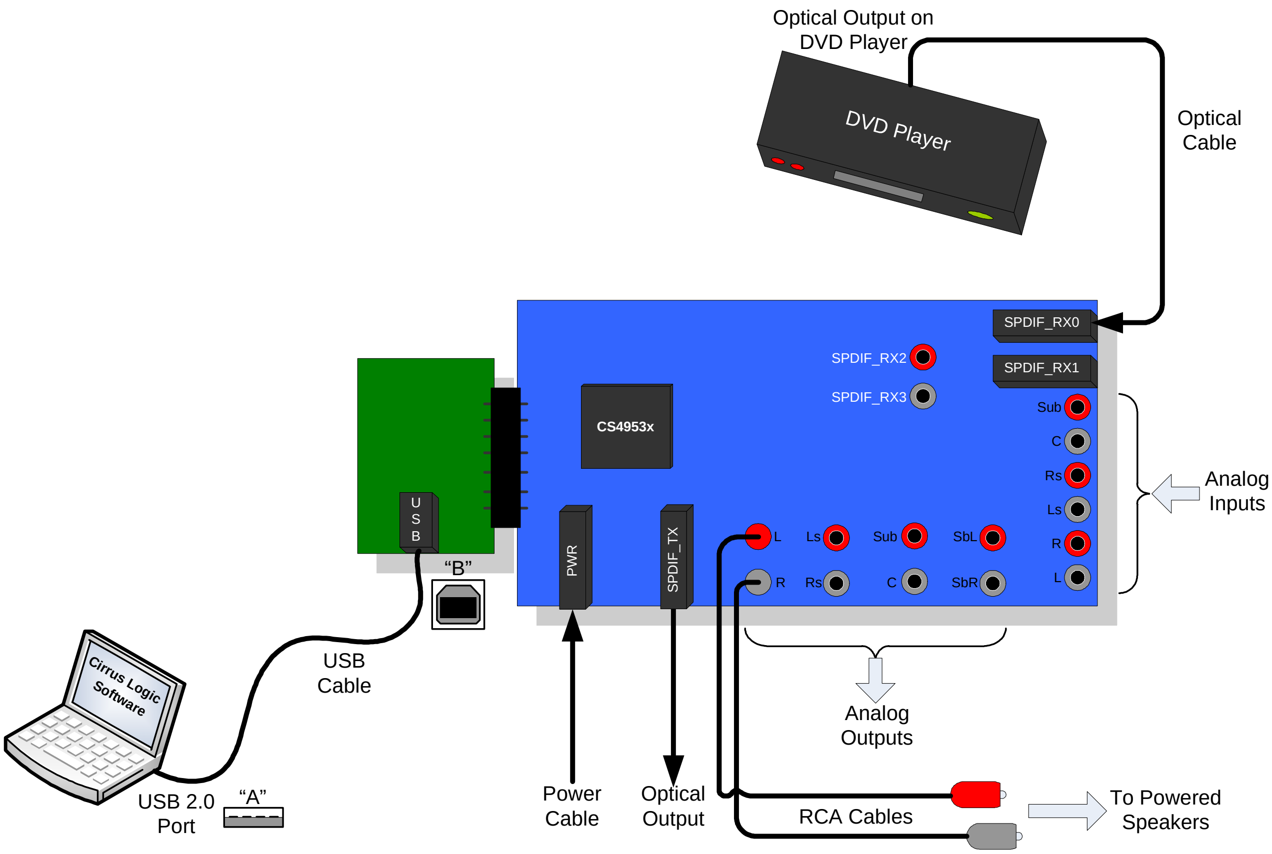


Figure 3-2. Board Setup Diagram

3.1.3 Connecting to a PC

1. Connect the "B" end of the USB cable to P1 on the CRD USB Master Digital I/O Card.
2. Connect the "A" end of the USB Cable to a USB 2.0 port on a notebook or PC running Win XP.
3. Windows should recognize that a new device has been attached and display a notice saying *"Found New Hardware"*.



Figure 3-3. ound New Hardware Window

4. Windows will display the *Found New Hardware Wizard* (below). Select the *No, not at this time* radio button so that Windows does not connect to Windows Update for the drivers. Click *Next*.



Figure 3-4. Found New Hardware Wizard Window

5. Windows will then ask whether to use automatic installation or manual installation. Allow Windows to install the software automatically and click *Next*.

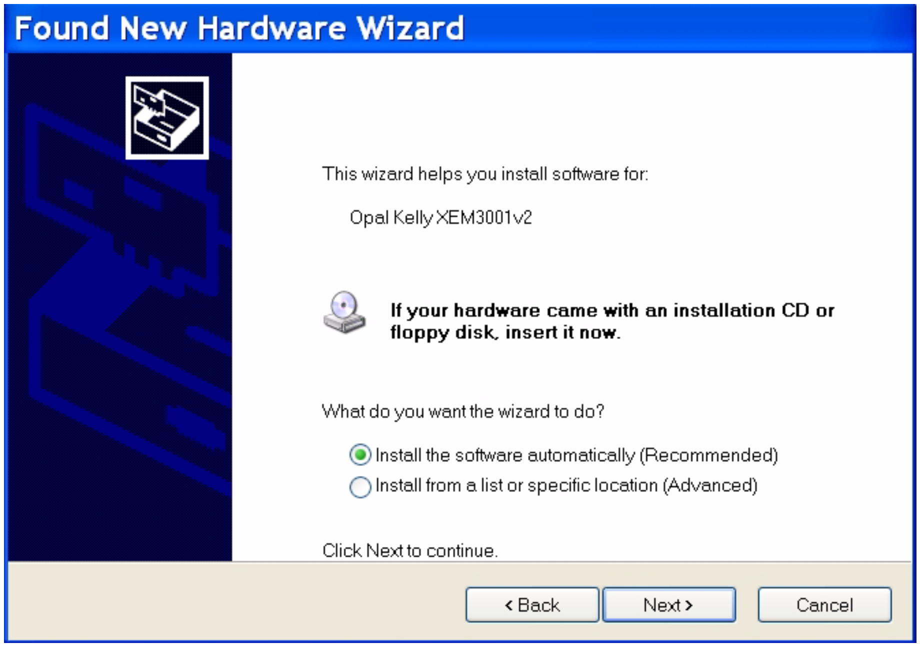


Figure 3-5. Found New Hardware Wizard with Automatic Installation Option Window

6. It is possible that during the installation, Windows might issue a warning that the drivers have not passed “Windows Logo” testing. Select *Continue Anyway*.

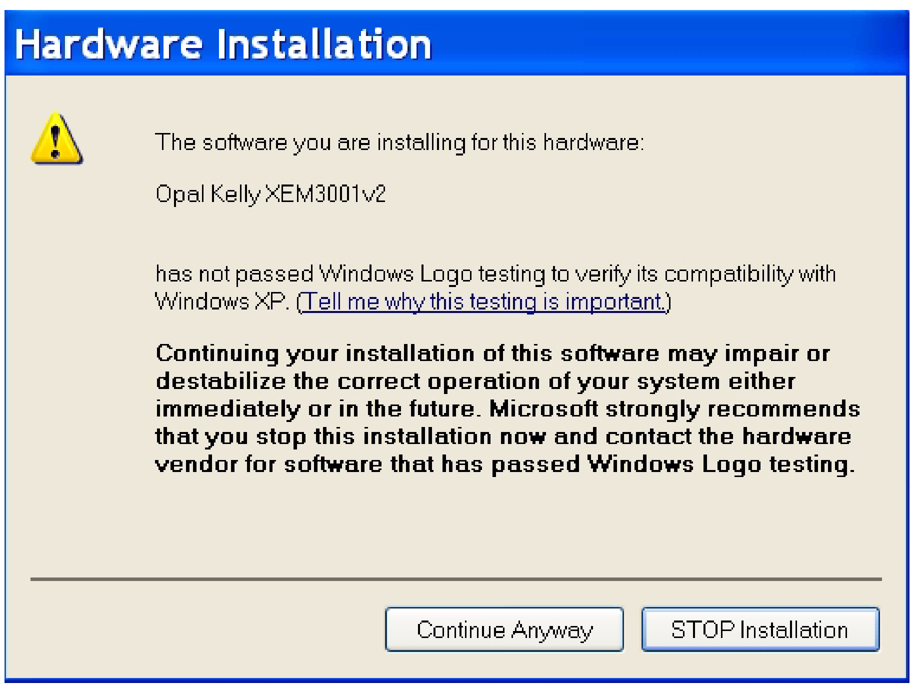


Figure 3-6. Hardware Installation Window

7. Windows should locate the correct drivers and complete the installation.

3.1.4 Running a Stereo PCM Application on CRD49530-USB

1. Launch DSP composer (*Start* ⇨ *Program* ⇨ *Cirrus DSP*).
2. In DSP Composer, go to *File* ⇨ *Open* and open *C:\CirrusDSP\CS4953X\projects\pcm_1fs.cpa.*
3. Press the *GO* button
4. Insert PCM material into the DVD player (e.g. music CD). If a DVD is being used as the audio source, make sure that the DVD Player (or other digital audio source) is configured to output PCM data.
5. Press *Play* on the DVD player (or other digital audio source). You should now hear audio from the speakers.

3.1.5 Downloading Other Applications

Separate project files (*.cpa*) are provided for other applications such as Dolby Digital. In order to evaluate these, please contact your local FAE to ensure that the necessary licensing agreements have been completed.

§§

Chapter 4

Programming the CRD49530-USB Board

4.1 Introduction

With the exception of the power selection jumpers, the CRD49530 is configured exclusively through software. The DSP Composer™ software is a graphical user interface (GUI) that is used to program the CS4953xx DSP, and to configure the CRD49530. This section provides basic instruction for using the GUI to control the CRD49530, but detailed information can be found in the DSP Composer™ User's Manual. Both the DSP Composer™ software, and the User's Manual for the software package will be provided by your local Cirrus Logic representative.

4.2 Basic Application Download and System Configuration - PCM Pass-through

Follow the instructions in "Installation, Setup, and Running First Application"on page 3-1 in order to install the USB drivers on your PC and launch CS4953x version of DSP Composer (the GUI used to control the CRD49530).

After following the instructions in "Running a Stereo PCM Application on CRD49530-USB"on page 3-6, the DSP Composer main window will appear as shown in Figure 4-1.

Figure 4-1 shows the DSP Composer™ main window for a PCM pass-through application on the CRD49530. The blocks shown in the main window of DSP Composer can be selected from the folders in the left-hand window pane, and then connected together by "wires" to indicate the processing path as shown.

The "Audio In" and "Audio Out" blocks represent the hardware ports that need to be configured. The "Audio In" block is used to select the S/PDIF Input or Analog input that is to be processed, and configure the digital audio format for the CS8416, CS42448 ADCs, and the CS4953xx DAI port. The "Audio Out" block is used to configure the digital audio format for the CS4953xx DAO port, the CS42448 DACs, and enable or disable the S/PDIF TX output of the CRD49530.

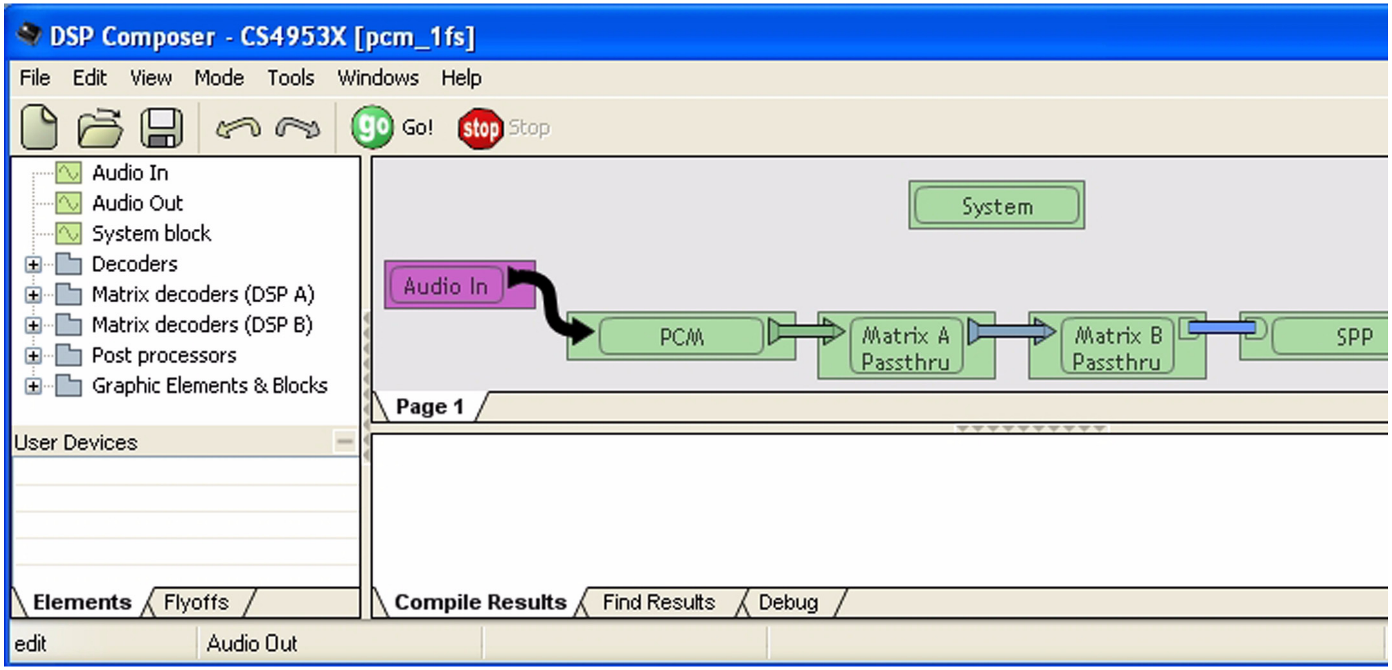


Figure 4-1. PCM Pass-through Example Application

4.2.1 System Block

In DSP Composer, when you drag the System block onto the work space, a pop-up menu is displayed. as illustrated in Figure 4-2. This menu offers the option of selecting the *Target chip* that you need to evaluate, the *Firmware version* and the *PCM input mode* from the pull-down menu.

.

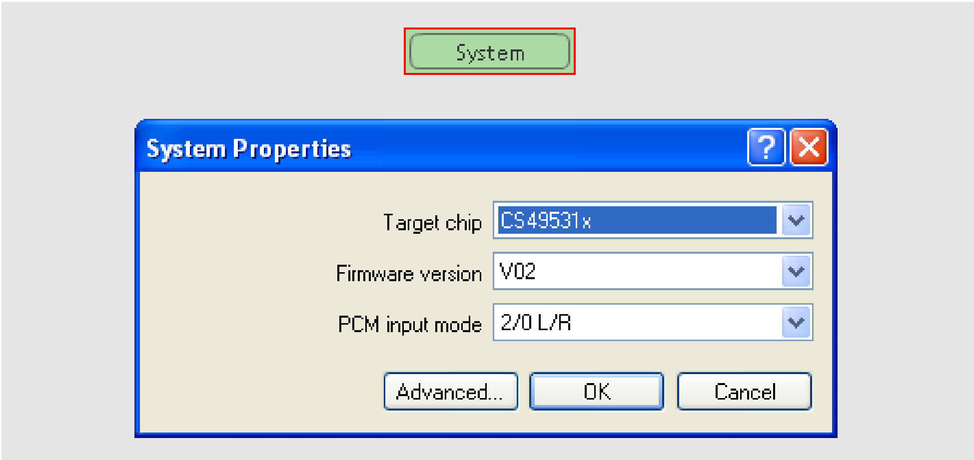


Figure 4-2. CRD49530 System Properties

4.2.2 Channel Remap of CS4953xx

The audio output channels of the CRD49530 can be mapped by double-clicking on the System block in DSP Composer.

Select the DAO remap tab as illustrated in Figure 4-3 and click on the DAO1 Combo Box to select the internal channel to route to DA01 channel.

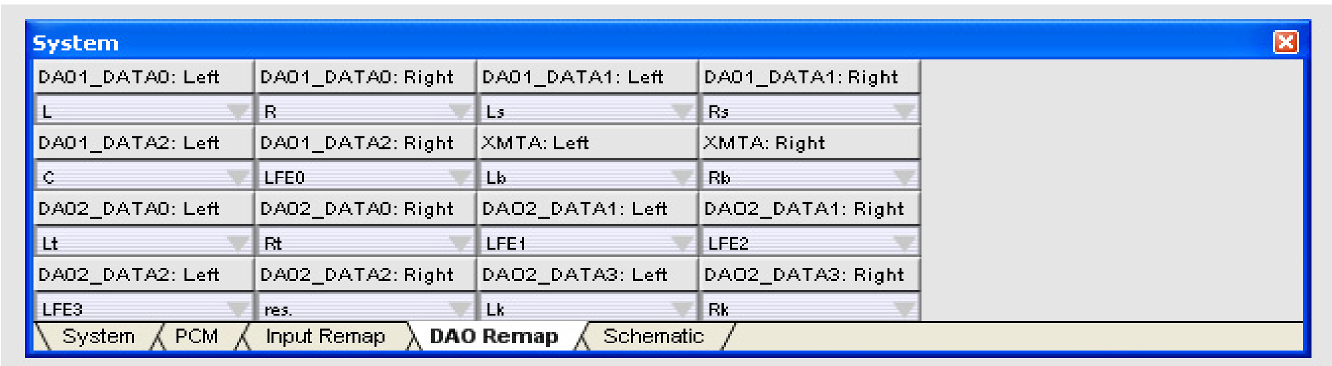


Figure 4-3. CRD49530 DAO Channel Remap

4.3 Changing Audio Input Source

The active audio input to the CRD49530 is selected through the "Audio In" block in DSP Composer, this is done by right-clicking on the "Audio In" block and selecting *Device Properties*, as illustrated in Figure 4-4.

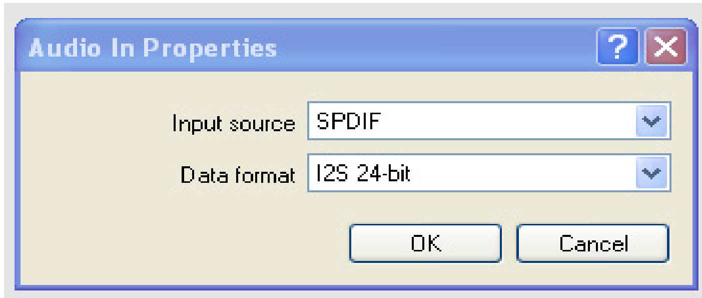


Figure 4-4. CRD49530 Audio In Properties

This dialog allows the user to set the following parameters for the CS4953xx:

- Input Source - S/PDIF, Analog or USB
- Audio Data Format - I²S, LJ, etc.

4.3.1 S/PDIF Audio Input

The CRD49530 has four different S/PDIF input jacks. The active S/PDIF input is selected using the SPDIF RX *Device Properties* dialog box in DSP Composer, as illustrated in Figure 4-5. Double-click on the "Audio In" block, then select the SPDIF block. Right-clicking the SPDIF block and selecting *Device Properties*, will display the *SPDIF Rx Properties* dialog.

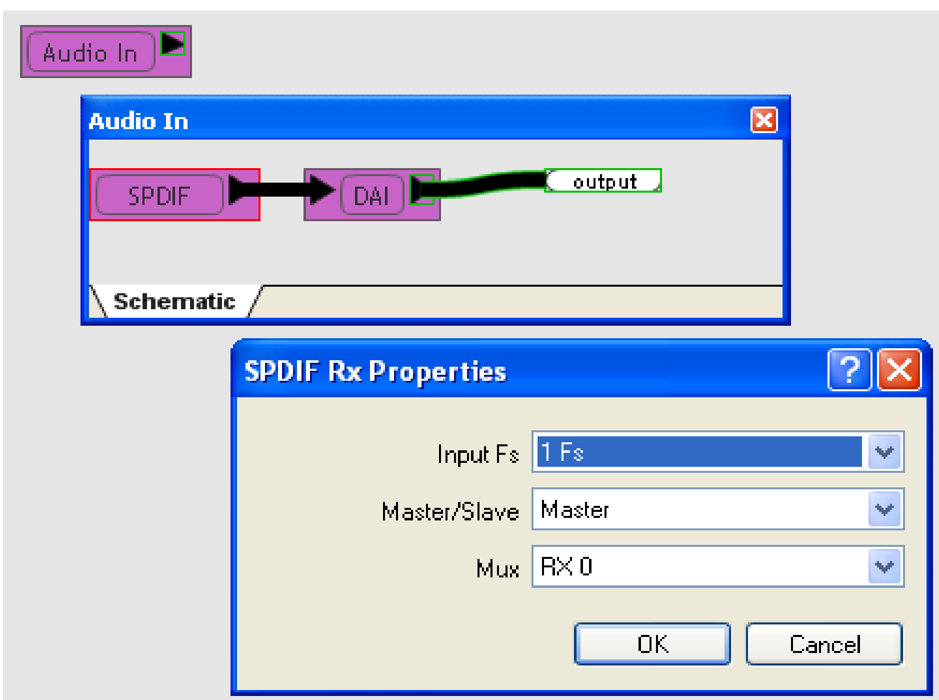


Figure 4-5. CRD49530 S/PDIF Rx Properties

4.3.2 Analog Audio Input

To deliver data to the DSP via 6ch ADC, drag the Audio In block to the work space and select "Analog" as the Input Source. Double click the Audio In block to see the signal flow. The *Device properties* of the Analog element lets you select the sampling frequency of the ADC on the CS42448 CODEC. The Master/Slave property must always be set to Master to indicate that the ADC will master SCLK and LRCLK as described in Section 1.3.10 "Audio Clocking" on page 1-6. The Audio In module with Analog as the input source is illustrated in Figure 4-6.

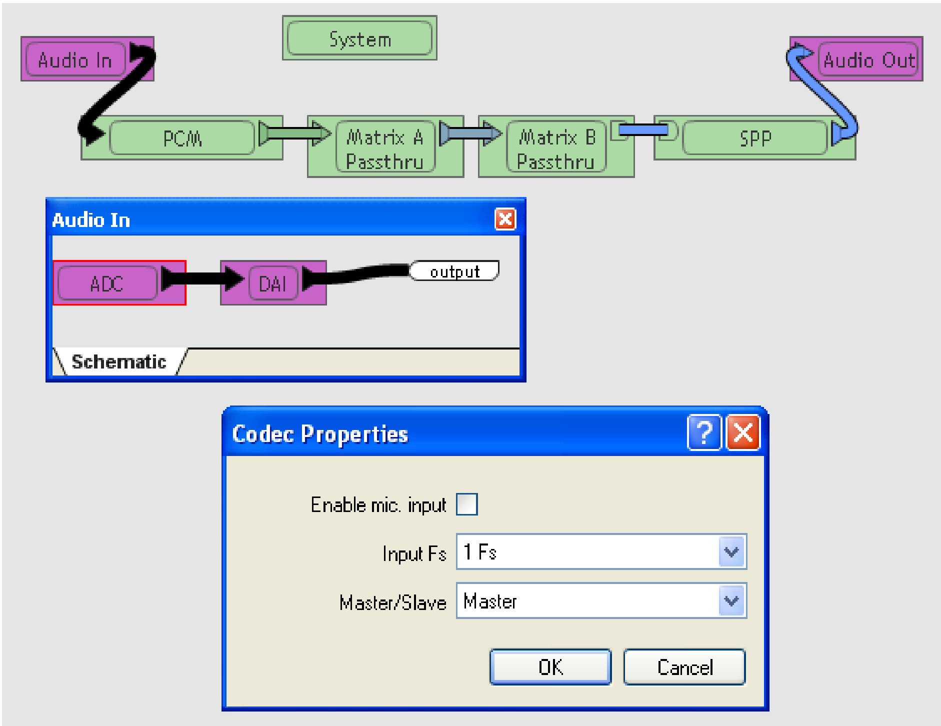


Figure 4-6. CRD49530 Analog Properties

This S/PDIF and Analog dialog allows the user to set the following parameters:

- Input and Output Sampling Frequency Range - Select the Fs range where
  - 1FS = 32 kHz, 44.1 kHz, or 48 kHz
  - 2Fs = 64 kHz, 88.2 kHz, 96 kHz
  - 4FS= 128 kHz, 176.4 kHz, 192 kHz
- Master/Slave settings for the SCLK & LRCLK pins on the CS8416. Set to Master when using S/PDIF input.
- SPDIF Mux: RX0 - RX3, and 'NONE'. Choosing 'NONE' forces the CS8416 to pass the DSP clock that comes in on the OMCK pin to MUXED_MCLK (RMCK). Use this setting when using the ADC.
- Analog Only - Enable microphone input.

4.3.3 USB (I^2S) Audio Input

This feature is used for debugging and development purposes via the usb_play utility.

4.3.4 DAI Input

Each available audio source for the board is shown as a block connected to the DAI port of the CS4953xx as illustrated in Figure 4-7. Right-clicking any of the sources and selecting *Device Properties*, produces the *DAI Properties* dialog.

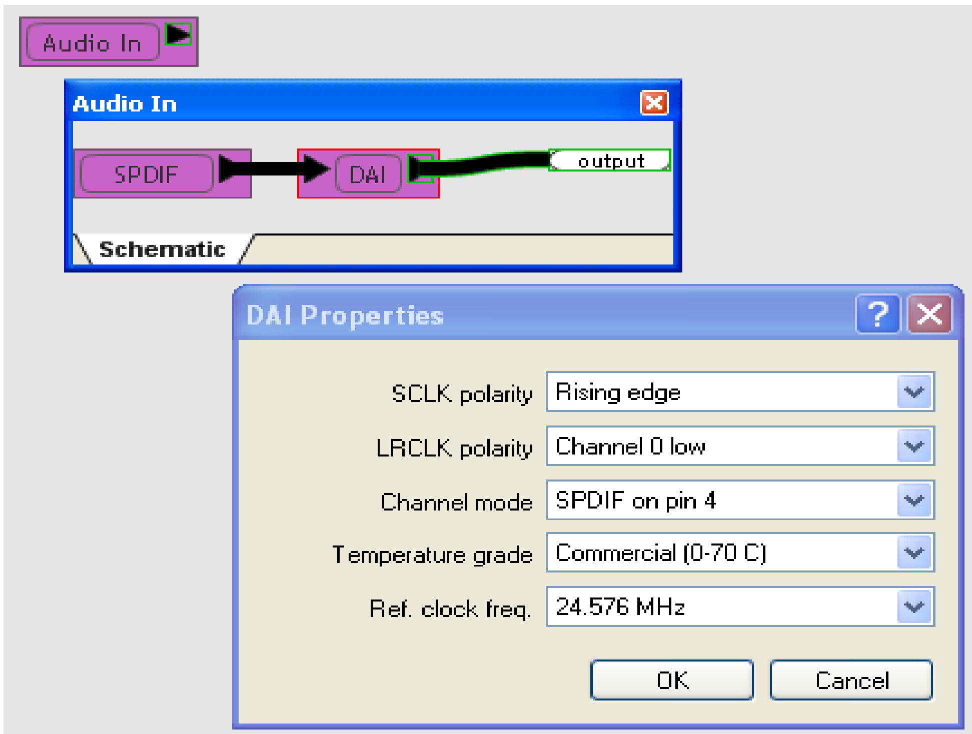


Figure 4-7. CRD49530 DAI Input Properties

This dialog allows the user to set the following parameters for the CS4953xx:

- SCLK polarity - Rising edge / Falling edge
- LRCLK polarity - Channel 0 low / Channel 0 high
- Channel Mode - SPDIF on pin 4 / SPDIF on pin 0
- Temperature Grade - CRD49530s are populated with commercial-grade chips by default
- Ref Clock - Set to the frequency of the crystal driving the CS49353xx (Y1). This is the reference clock is used to determine the clock dividers needed to derive Fs in ADC-only applications. If this number changes, then all dividers for LRCLK/SCLK will change by the same ratio (e.g. @24.576 MHz MCLK/512 = 1Fs = LRCLK, @12.288 MHz MCLK/256 = 1Fs = LRCLK)

4.4 Changing Audio Output Source

The audio output section of the CRD4930 is configured through the "Audio Out" block in DSP Composer, this is done by right-clicking on the "Audio Out" block and selecting *Device Properties*, as illustrated in Figure 4-8.

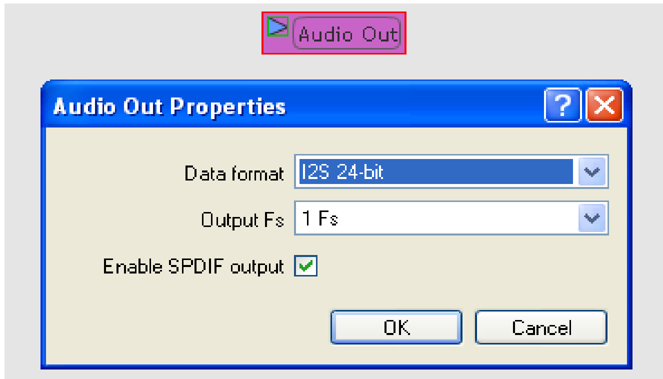


Figure 4-8. CRD49530 Audio Out Properties

This resulting dialog allows the user to set the following parameters for the CS42448 DACs:

- Audio Data Format - I^2S, LJ, etc.
- Output Sampling Frequency Range - Select the Fs range where 1FS = 32 kHz, 44.1 kHz, or 48 kHz, 2Fs = 64 kHz, 88.2 kHz, 96 kHz, 4FS= 128 kHz, 176.4 kHz, 192 kHz, etc.
- SPDIF Enable - Checking this box configures DAO for S/PDIF output rather than I^2S.

4.4.1 DAO Output of CS4953xx

The digital audio output (DAO) of the CS4953xx is very flexible, making it compatible with a wide variety of audio devices. This port can configured using the dialog box shown in Figure 4-9. Double-click on the "Audio Out" block, then select the DAO block. Right-clicking the DAO block and selecting *Device Properties* produces the *DAO Properties* dialog.

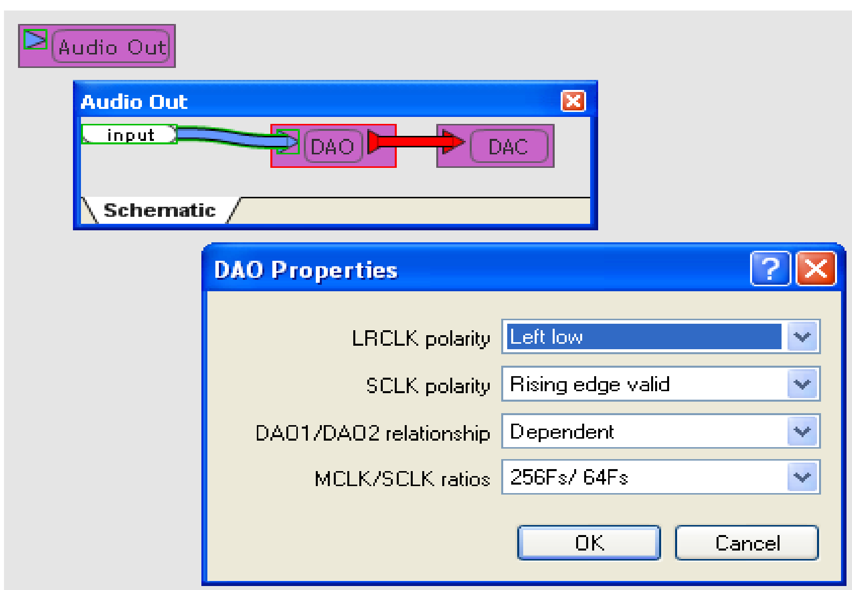


Figure 4-9. CRD49530 Digital Audio Output Properties

This dialog allows the user to set the following parameters for the CS4953xx Audio Output:

- LRCLK polarity - Select the phase of LRCLK when the left-sample will be shifted out.
- SCLK polarity - Select which edge of SCLK for which the output data will be valid.
- DAO1/DAO2 - Select independent or unified clock domains for the DAO1 and DAO2 audio output ports.
- MCLK/SCLK Ratios - Select the ratio of LRCLK to MCLK, and LRCLK to SCLK.

4.4.2 Changing Serial Control Protocol (I^2C® or SPI™) / Memory Usage

The CRD49530 is designed to communicate using either I^2C or SPI protocols. In order to change the communication mode in DSP Composer go to the menu bar and select *File ⇨ Properties*, which brings up the *Project Properties* dialog. To configure Memory usage click on the *Advanced* button, as illustrated in Figure 4-10; Max memory allocation and external memory can be enabled from this panel.

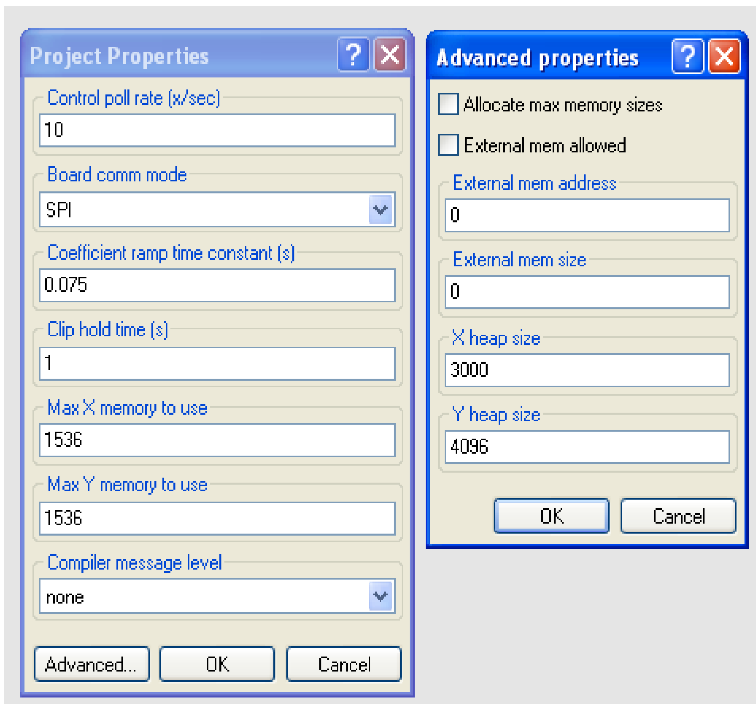


Figure 4-10. CRD49530 Comm Mode / Memory Usage

4.5 Programming the On-board Serial Flash

The CRD49530 is populated with 4 Mbits of serial Flash that can be used to store custom DSP firmware or run-time firmware configuration options. In order to emulate a system that boots the DSP from Flash, the serial flash can be programmed in system with the desired DSP firmware. The host (the PC in this case) can be used to perform a host-controlled master boot (HCMB) to boot the CS4953xx.

A special *.uld* file is loaded into the CS4953xx which provides the programming interface to the system host. Programming then becomes a sequence of messages to the CS4953xx.

Please contact your local Cirrus representative for the Flash programming *.uld* file and the associated application note.

§§

Chapter 5

CRD49530-USB Schematics

5.1 Introduction

The schematics included in this document are the original Revision A schematics of the CRD49530 and reflect the board as it was manufactured. Newer schematics may be available which incorporate feature additions or corrections, and may not reflect Rev. A hardware.

5.2 Detailed Schematic Descriptions

5.2.1 CS49530-USB Block Diagram

Figure 5-1 shows the CRD49530-USB block diagram.

5.2.2 CS4953xx DSP

The schematic for the CS4953xx core is shown in Figure 5-2. The DSP core is driven by an external crystal circuit. This fixed 24.576 MHz clock is buffered and driven out the XTAL_OUT pin of the CS4953xx chip and can be used as the audio MCLK for analog sampling in the CS42448 codec.

The PLL filter circuit on the CRD49530 is designed to allow the use of the CS4953xx family of DSPs and the legacy CS495xx DSPs. The board is configured for the CS4953xx PLL by default, but extra components can be populated to support the CS495xx as explained by the note on the bottom of the schematic page.

The DSP has a dedicated reset line (DSP_RESET) that must be driven by the host to initialize the CS4953xx's communication mode and initiate the first boot sequence. This signal is independent of any other reset on the board and can be used to sequence device power up.

The host communication protocol of the DSP is determined by the state of the HS[3:0] pins at the rising edge of reset. The communication mode for the CRD49530 is slave-I^{2}C when the SPI_MODE_SEL signal is driven low, and slave-SPI when the SPI_MODE_SEL pin is driven high.

The serial host control port (SCP1_CLK, SCP1_MOSI, SCP1_MISO/SDA, SCP1_CS, SCP1_IRQ, SCP1_BSY) is used by the host controller to boot and control the DSP. Note that the pull-up resistors on the SCP1_IRQ and SCP1_BSY pins are required for both SPI and I^{2}C control, since these are open-drain pins. The pull-ups on the SCP1_CLK and SCP1_SDA pins are required only for I^{2}C operation.

The second serial control port (SCP2CK, SCP2_MOSI, SCP2_MISO, EE_CS) is connected to the on-board serial SPI flash chip found on the memory page of the schematic.

The DSP has a debug port (DBDA, DBCK) that allows a developer to debug the DSP during normal operation. This is a slave port that can be connected to an I^{2}C master, or it can be simply terminated with pull-up resistors.

The audio input pins of the CS4953xx are driven by a multiplexer (U1, U2) that chooses between I^{2}S audio from an off-board source (HDMI audio) and the on-board S/PDIF RX (CS8416) and audio codec (CS42448). This multiplexer defaults to choose the on-board audio sources. The HDMI audio delivery interface is currently under development.

The input and output audio clocking domains are separated. This allows the DSP to accept audio in one Fs and produce output samples at a different sample rate such as 2Fs or 4Fs. The CS4953xx is slave only on the input clock domain (MUXED_SCLK, MUXED_LRCLK). On the audio outputs, the CS4953xx is slave-only for the MUXED_MCLK master audio clock, and master-only for DSP_SCLK and DSP_LRCLK which are used to shift data out of the CS4953xx.

The CRD USB Master USB board acts as the host controller in the CRD49530 platform, and is connected to the CRD49530 via J11 on page 8 of the schematics. The CRD USB Master drives several DSP interfaces including the serial host control port (SCP1), the debug port, and DSP_RESET. The CRD USB Master also controls the multiplexer (ADC/HDMI_SEL) that selects the I^2S audio input lines for the CS4953xx.

5.2.3 Memory

Figure 5-3 shows the schematic for the SDRAM and Flash memory blocks. The CRD49530 was designed with 4 Mbit of serial flash on-board. Both standard serial flash footprints are supported in this design, and this is shown in the schematic as two different serial flash devices. By default, only the SST flash (U13) is populated

The CRD49530 is populated with a 64 Mbit, 166 MHz SDRAM with a 16-bit-wide data bus (U7). Note that both the series termination (R40) and the parallel termination (R42) for SD_CLKIN are physically close to the DSP on the board. Both termination options were designed into the CRD49530, but only the parallel termination is being used on this board, so the series terminator (R40) is populated with a 0-ohm resistor.

Note: SA_BA1 is the default bank address for 16-Mbit SDRAM designs. SD_BA1 and SD_BA0 are swapped in the CRD49530-USB design to allow for the evaluation of both 16-Mbit and 64 M-bit designs. SD_BA1 and SD_BA0 do not need to be swapped for 64-Mbit designs.

The parallel flash (U6) is not populated. serial Flash is recommended for all CS4953xx systems, as it makes layout of the SDRAM interface much simpler, but the parallel flash footprint has been included as an option.

5.2.4 S/PDIF Receiver

Figure 5-4 shows the schematic for the CS8416, which is a S/PDIF receiver capable of supporting sample rates up to 192 kHz.

The serial host control port (SCL/CCLK, SDA/CDOUT, AD1/CDIN, AD0/CS) shares clock and data lines with the CS4953xx and CS42448. The CS8416_CS line is unique to this chip and driven only when in SPI mode. The pull-ups required for the SCL and SDA pins are shared with the other devices on the CRD49530 board.

The BRD_RST signal is a shared reset signal.

The reference clock for the CS8416 is the XTAL_OUT (buffered 24.576 MHz crystal) output from the CS4953xx.

The CS8416_MCLK signal is the master audio clock for on-board audio sources. This clock can be either an MCLK recovered from a S/PDIF stream or the XTAL_OUT reference, depending on the setting of the CS8416's internal multiplexer.

The CS8416 is master only for the CS8416_MCLK signal, which is one possible source for the MUXED_MCLK master audio clock.

The CS8416 slaves to the CS8416_SCLK and CS8416_LRCLK signals which are used to shift I^2S data out of the CS8416 and shift I^2S data into the CS4953xx.

The CS8416 has 5 different S/PDIF inputs available to it. Its internal multiplexer is used to select the active source.

A general-purpose output of the CS8416 is used to generate an independent reset signal for the CS42448 audio codec. Providing a separate reset line for each audio device allows the system to sequence the order in which audio devices come out of reset.

The CRD USB Master USB board acts as the host controller in the CRD49530 platform, and is connected to the CRD49530 via J11 on page 8 of the schematics. The CRD USB Master drives the serial host control port and $\overline{\text{CS8416_RESET}}$ signals on this page.

5.2.5 Audio CODEC

Figure 5-5 shows the schematic for the CS42448, which is a multi-channel ADC/DAC that is capable of simultaneously supporting up to 6 channels of analog input and 8 channels analog output.

The serial host control port (SCL/CCLK, SDA/CDOUT, AD1/CDIN, AD0/$\overline{\text{CS}}$) shares clock and data lines with the CS4953xx and CS8416. The $\overline{\text{CS42448_CS}}$ line is unique to this chip and driven only when in SPI mode. The pull-ups required for the SCL and SDA pins are shared with the other devices on the CRD49530 board.

The $\overline{\text{CS42448_RST}}$ signal is a dedicated reset signal driven by a general-purpose output of the CS8416.

The CS42448 is a slave to the MUXED_MCLK signal, which is the master audio clock for the entire CRD49530 system.

The CS42448 masters the CS8416_SCLK and CS8416_LRCLK signals which are used to shift I^2S data out of the CS42448 and shift I^2S data into the CS4953xx.

The CS42448 slaves to the DSP_SCLK and DSP_LRCLK signals which are used to shift I^2S data out of the CS4953xx and shift I^2S data into the CS42448.

The analog inputs and outputs of the CS42448 are being used in single-ended mode. This is evident when looking at the input and output filter circuitry on page 6 of the schematics.

AIN5 of the CS42448 has an internal analog multiplexer that can be used to select between single-ended inputs on the AIN5+ and AIN5- pins. This feature is used to share AIN5 between the microphone input and RCA jack J27.

The transistor connected to MUTEC (Q1) provides the current drive necessary to drive all of the mute transistors (see page 6 of schematic) into saturation.

The CRD USB Master USB board acts as the host controller in the CRD49530 platform, and is connected to the CRD49530 via J11 on page 8 of the schematics. The CRD USB Master drives the serial host control port signals shown on this schematic page.

5.2.6 Input/Output Filters

Figure 5-6 shows the input and output filters for the CRD530_USB board. Each input of the CS42448 has its own input filter that consists of a voltage divider, an AC-coupling capacitor (10 µF), and a anti-aliasing capacitor (2700 pF). The voltage divider is provided to make the CRD49530-USB capable of accepting analog signals of up to 2 VRMS. The CS42448 analog inputs register full-scale for an input amplitude of 1 VRMS.

Each output of the CS42448 has an output filter that consists of an AC-coupling cap (3.3 µF), a pull-down resistor to prevent the output from floating when not connected to a load, a series resistor (470 Ω) to provide a voltage drop when the muting transistor is enabled, and a mute transistor that will pull the output low when the mute control signal is enabled. The series resistor is small enough that it does not affect the signal in normal operation, assuming a load of at least 10 kΩ is connected to the analog output of the board.

5.2.7 Microphone Preamplifier

Figure 5-7 shows the microphone preamplifier on the CRD49530-USB, which has a 1/8" microphone input jack to allow direct connection to an encapsulated condenser microphone (ECM). Because the output of the ECM is so small, a pre-amplifier is needed to boost the signal to a line-level voltage.

These specifications for the amplifier are noted on the schematic page. These parameters should be considered when choosing the microphone to be connected to the CRD49503-USB. Too large of a signal on the CS42448 analog input will result in distortion of the sampled signal.

It is important to note that although the amplifier circuit shown is non-inverting (the input to U12-B is the same polarity as the output from U12-C), the output of an ECM is inherently inverted since it acts as an open-collector device. Therefore the microphone signal driven to the CS42448 should be considered an inverted signal for processing purposes.

5.2.8 Power and Connectors

The audio input connectors consist of:

- 6 RCA jacks for analog input
- 2 RCA jacks for coaxial S/PDIF input
- 2 optical jacks for optical S/PDIF input

The audio output connectors consist of:

- 8 RCA jacks for analog output
- 1 optical jack for S/PDIF output

There is one control connector on the board, J11. This 50-pin connector provides pins for the following functions:

- Serial control interface for configuring the DSP, codec, and S/PDIF RX
- Reset lines for the DSP and other board devices
- Pins to provide power to the CRD USB Master USB control board
- An interface for delivering audio data from the USB board (feature not yet available)

The DC input connector (J25) for the CRD49530 can accept 9 to 12 VDC, and the power supply should be capable of supplying at least 1 amp of current.

The 3 voltage regulators on the CRD49530 generate the 1.8V, 3.3V, and 5V necessary for powering all of the ICs on the board. Note that the 5 V and 3.3 V regulators run directly off the DC input supply connected to the CRD49530, while the 1.8 V regulator is dependent upon 3.3 V system power (not necessarily the 3.3 V regulator).

The 3 power jumpers (J17, J18, J19) are used to choose between the on-board regulators, and an external source for 5 V, 3.3 V, and 1.8 V. This is a feature intended only for special applications, so these jumpers should be left in the 'REG' position for normal operation.

The DC input power jumper (J3) is used to bring the main 9 to 12VDC supply voltage from the control connector (J11) rather than the standard DC input connector (J25). This jumper is not populated on the board, and is intended only for special applications. J3 should not be used in normal operation.

5.3 Obtaining Schematic Updates

Updates to the schematics for the CRD49530 Development Board can be can be obtained from your local Cirrus Logic representative as part of a design package including the associated BOM, and layout artwork. The schematics are provided in Adobe's portable document format (PDF) and PADS™ format.

The schematics included in this document are the original Revision A schematics of the CRD49530 and reflects the board as it was manufactured. Newer schematics may be available that incorporate feature additions or corrections, and may not match Rev. A hardware.

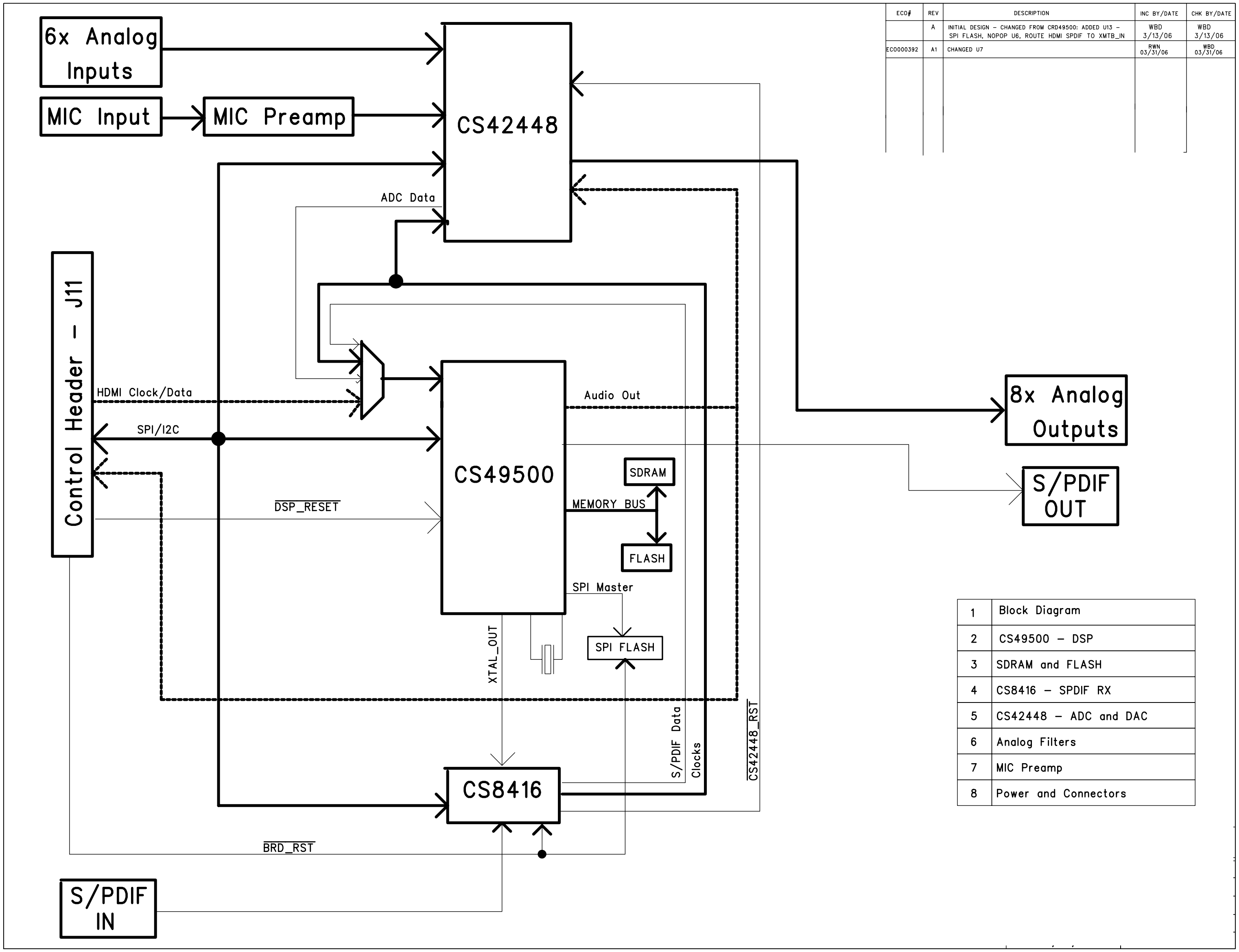
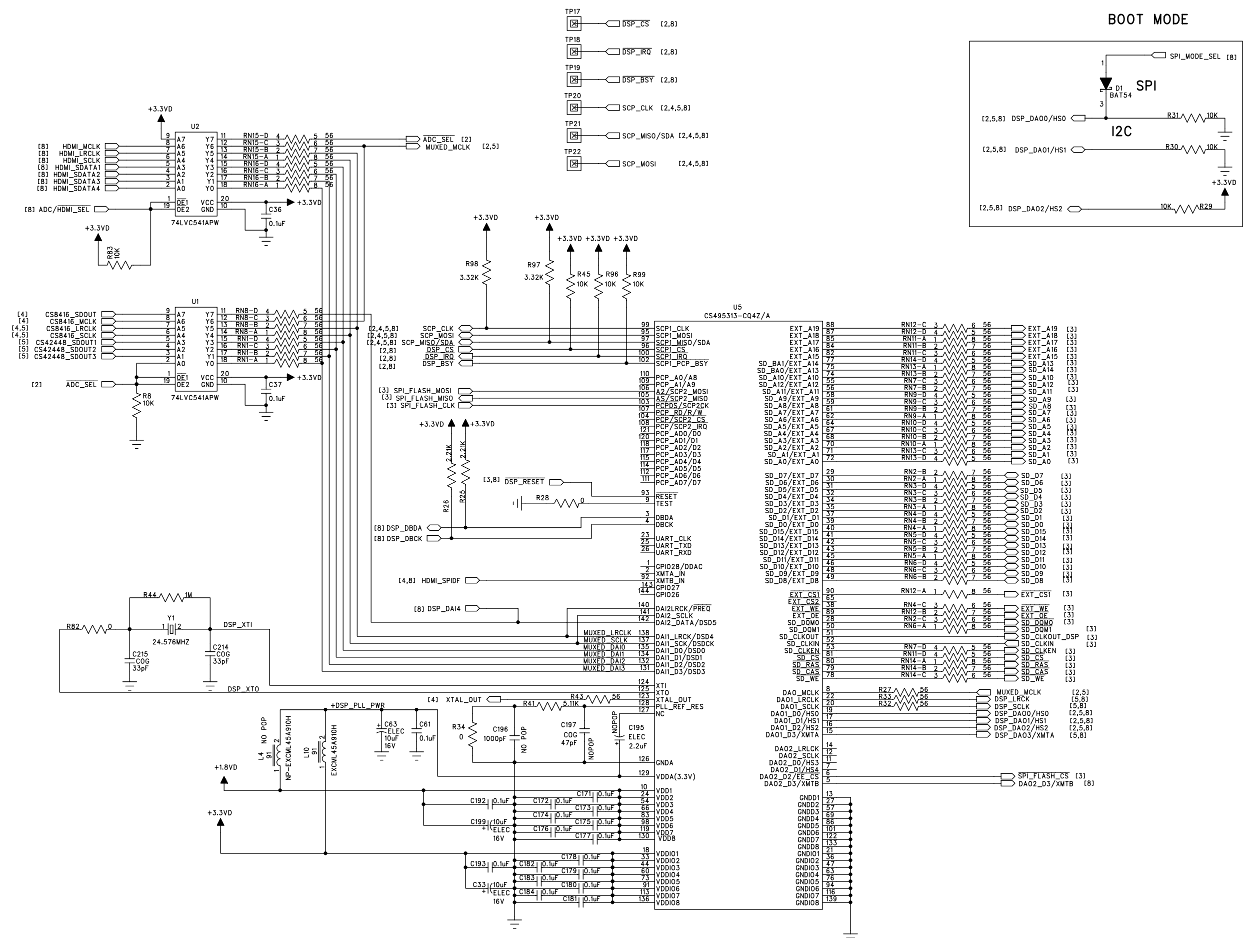


Figure 5-1. CRD49530-USB Block Diagram



NOTES: UNLESS OTHERWISE SPECIFIED;

1. ALL RESISTOR VALUES ARE IN OHMS.

DEFAULT SPI & I2C ADDR = 0x80

PLL CONFIGURATIONS

2. CS49500: L4 == POPULATED, L10 = NOPOP, R34 = NOPOP, R41 = 5.90K @1%, C195 == 2.2uF, C196 == 1nF COG, C197 == 47pF COG
3. CS49530X: L4 == NOPOP, L10 == POPULATED, R34 = 0 OHM, R41 = 5.11K @ 1%, C195 == NOPOP, C196 == NOPOP, C197 == NOPOP

Figure 5-2. CS49953xx DSP on CRD49530-USB Board

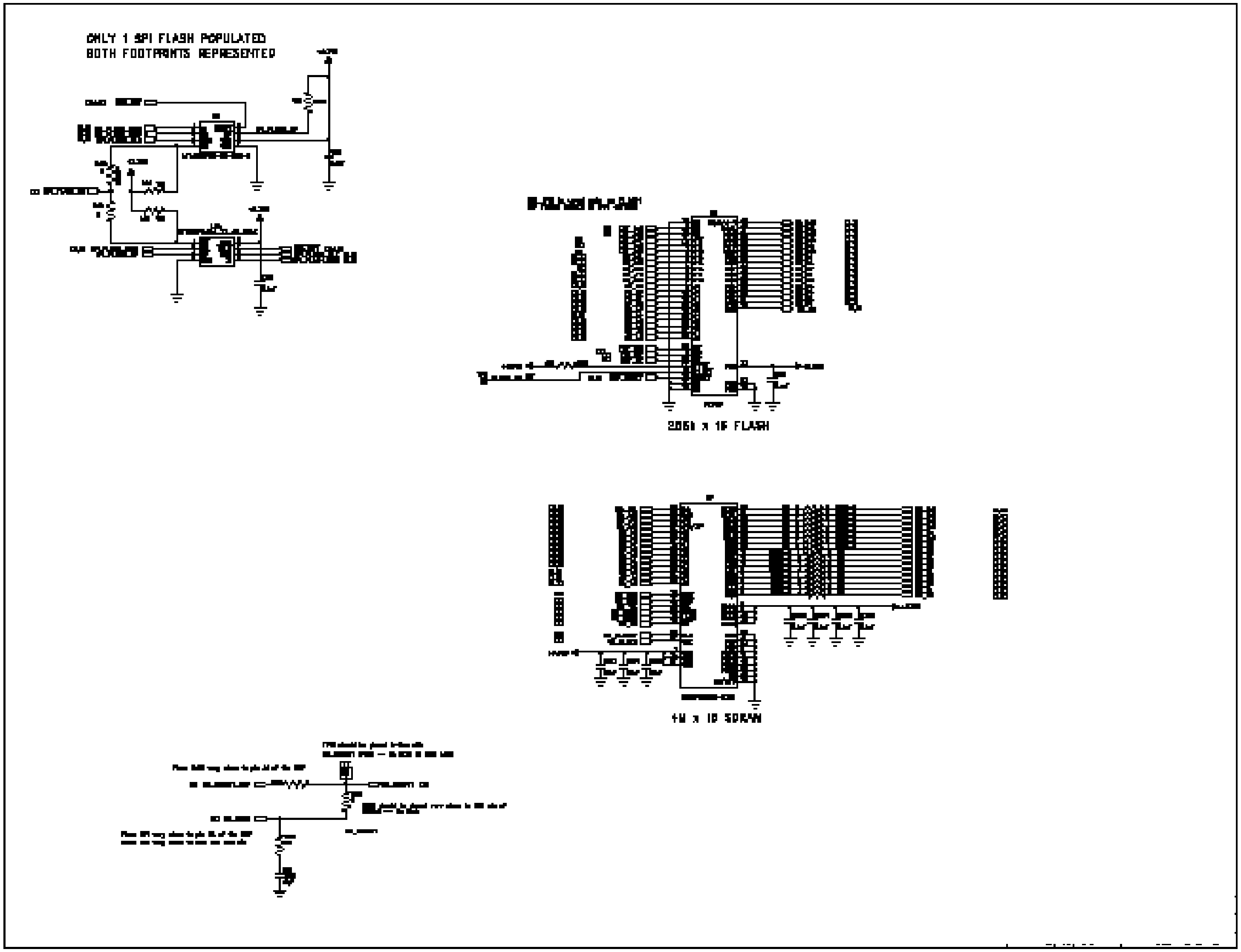


Figure 5-3. SDRAM and Flash Block

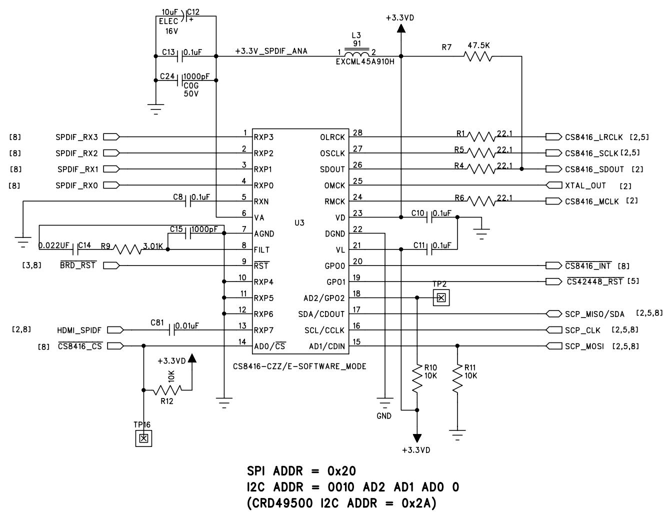


Figure 5-4. S/PDIF Receiver

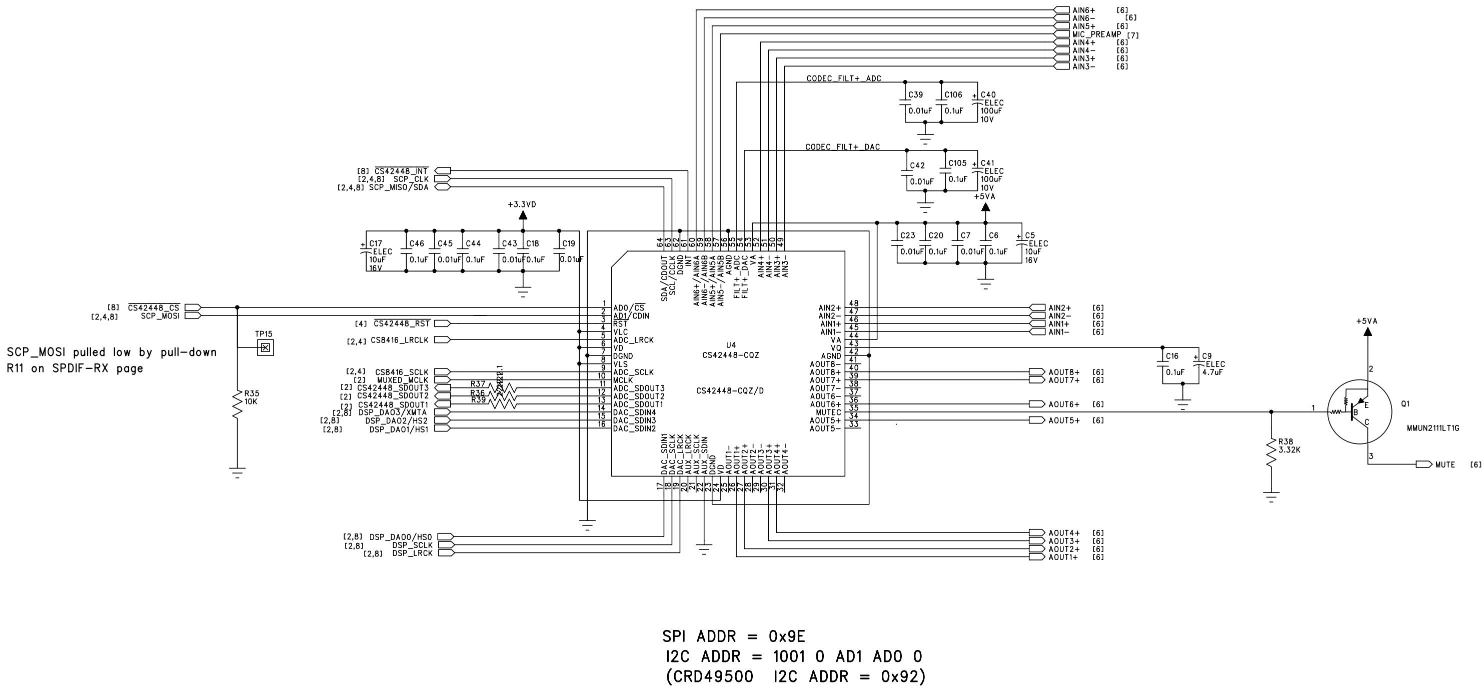


Figure 5-5. CS42448 CODEC

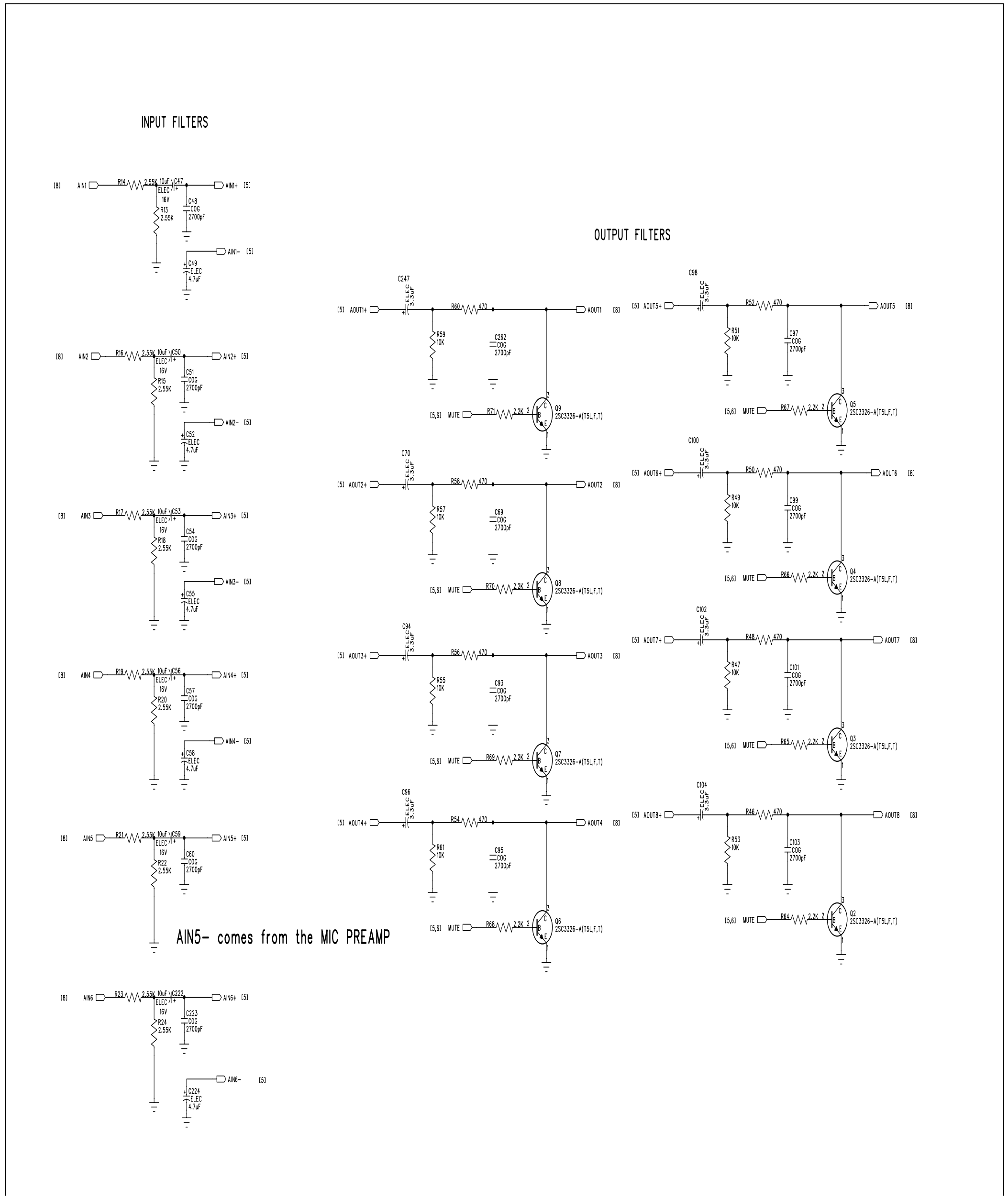


Figure 5-6. Input / Output Filters

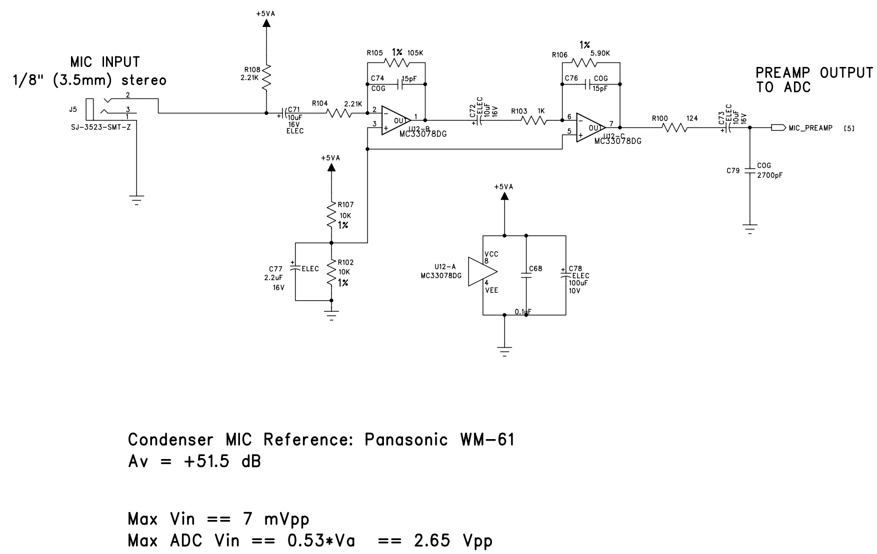


Figure 5-7. MIC Pre-AMP

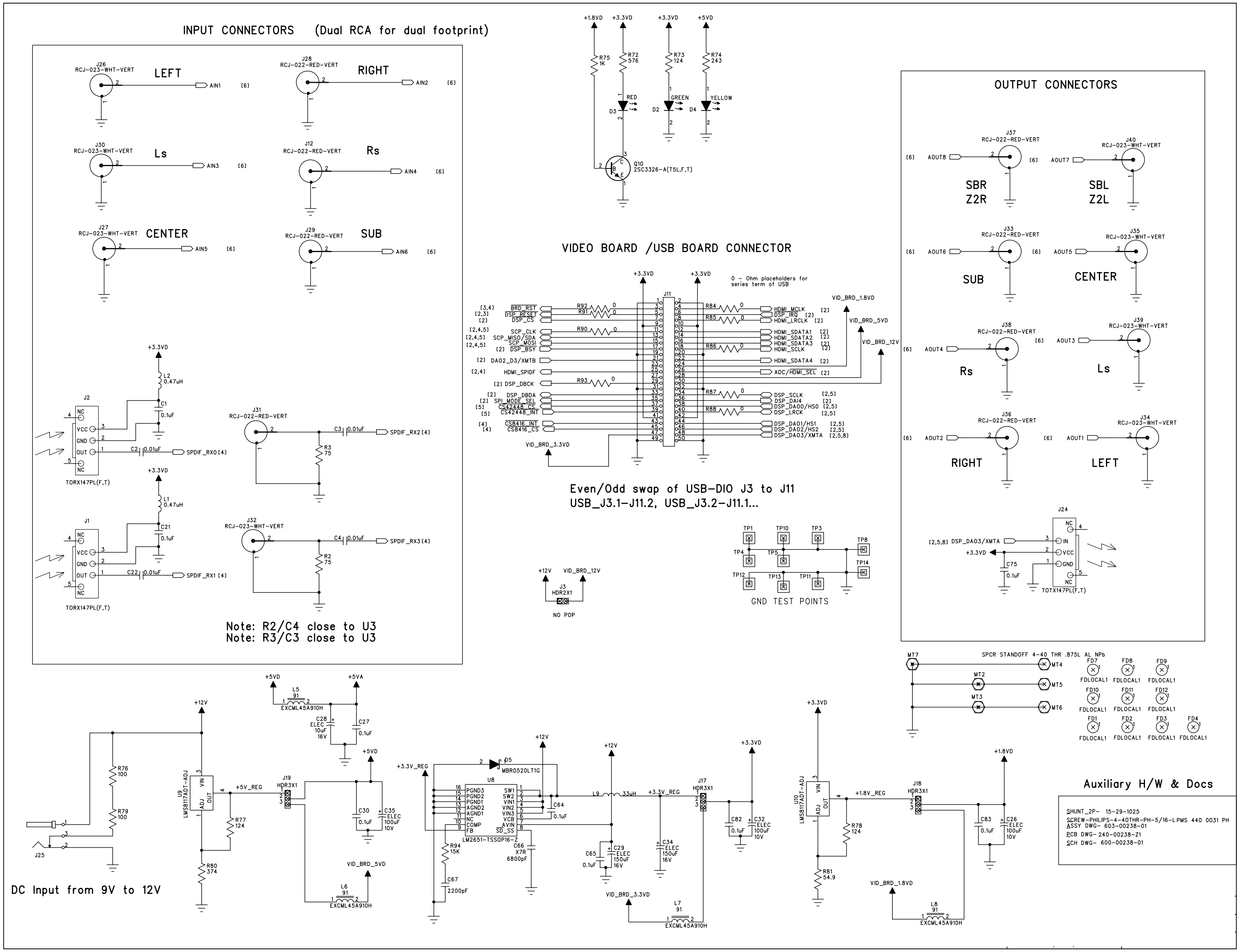


Figure 5-8. Connectors and Power

§§

Chapter 6

Troubleshooting

6.1 Troubleshooting Guide

This section provides solutions to problems that users might experience when using the CRD49530-USB.

6.1.1 Power LEDs

Problem: Power LEDs are not illuminated.

- Possible cause: **DC power supply is not connected to CRD49530-USB.**

  Solution: Ensure the DC wall supply is connected to the DC power input jack (J25), and the supply is plugged into a wall outlet.

- Possible cause: **Power selection headers (J17, J18, J19) are set incorrectly.**

  Solution: If you are using the DC wall supply provided with the CRD49530-USB, all jumpers should be in the 'REG' position.

- Possible cause: **Jumper settings when using an external power supply are set incorrectly.**

  Solution: If you are using an external power supply for any of the system voltages (5V, 3.3V, 1.8V), ensure that the jumper for that voltage has been removed and power is applied to the center pin of the appropriate header.

6.1.2 Board not Recognized by PC

Problem: CRD49530-USB is not Recognized by PC

- Possible cause: **DC power supply is not connected to CRD49530.**

  Solution: The CRD49530 is not a USB-powered device. Make sure the DC wall supply is connected to the DC power input jack (J25), and the supply is plugged into a wall outlet.

- Possible cause: **CRD49530 USB Drivers not installed before connecting to PC**.

  Solution: Follow these steps:

  1. Pull the DC power plug on the CRD49530.
  2. Open the device manager on the PC and search for the "Opal Kelly" device under "USB Devices".
  3. If there is a question mark next to the device, right click on it and open "Properties." Press the "Update Driver" button and let Windows automatically find the driver.
  4. Wait 3 seconds, and plug the DC power supply back in.

6.1.3 Audio is not Heard

Problem: Audio cannot be heard.

Possible cause: **S/PDIF Source is not connected to RX0.**

Solution: Follow the instructions in "Running a Stereo PCM Application on CRD49530-USB" on page 3- 6. If the sound still cannot be heard, connect the audio source to RX0, or change the S/PDIF input to the appropriate connector according to the instructions in "USB (I2S) Audio Input" on page 4- 5.

6.1.4 Only Stereo Audio is Heard

Problem: Only Stereo Audio is heard even when delivering a multi-channel compressed audio stream (e.g. Dolby Digital, DTS).

Possible cause: **DVD Player is not configured properly.**

Solution: DSP is auto detecting a PCM stream and playing the 2-channel PCM. Navigate to the audio setup for the DVD player and set to “Bitstream Out” instead of “PCM Out.”

Revision History

Revision	Date	Changes
RD1	JUN 2006	First release.
RD2	DEC 2007	Update DSP Composer information. Updated Figure 5-2, "CS49953xx DSP on CRD49530-USB Board" on page 7. Added note to Section 5.2.3 “Memory” on page 5-2. Removed Cirrus Corporate address information from page 2. Use the URL for the Cirrus Logic Website located in the legal notice on this page to obtain the latest Cirrus Logic ontact information .Replaced “technical reference manual” and replaced it with “User’s Manual” to match current documentation style practices.
RD1	September 8, 2008	Reformatted manual into current style practices. Reorganized content into Chapters with page numbers in the <chapter>-<page number> format. Changed document number from DS732RDx to DS705RDx to match the numbering schema for the data sheet for the CS4953xx product.

§§